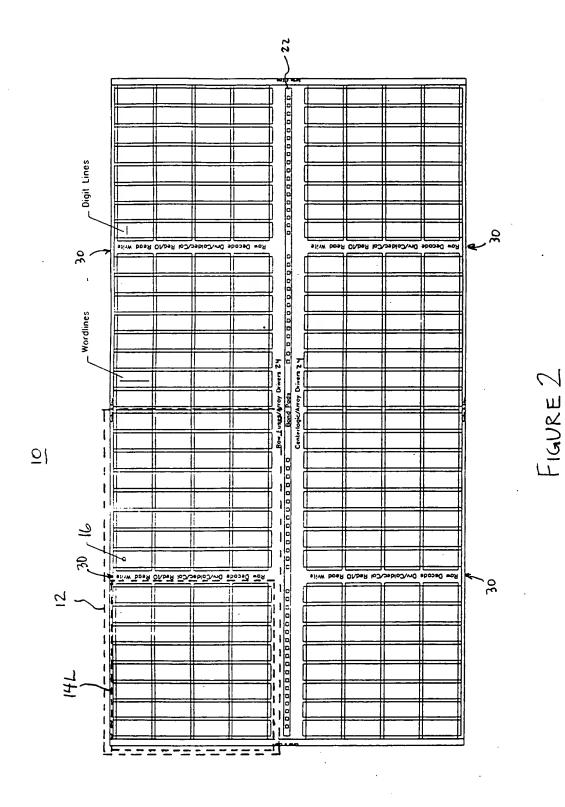


<u>II —</u> I PRIDR ART

į.

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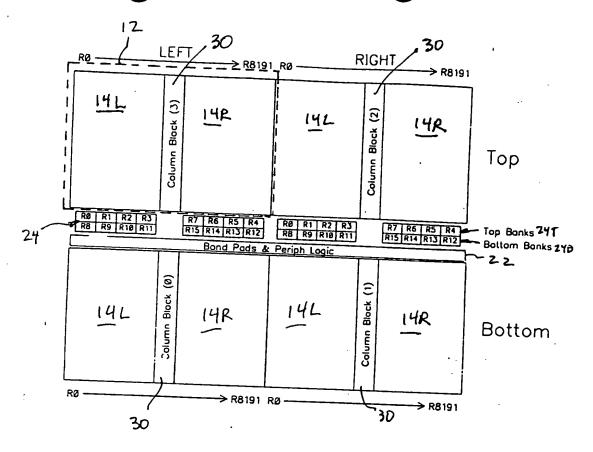


FIGURE 3

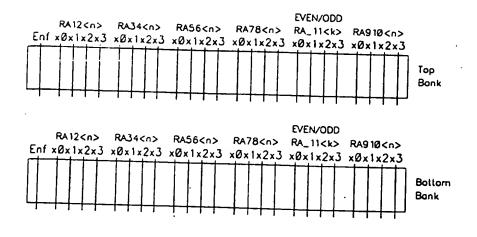
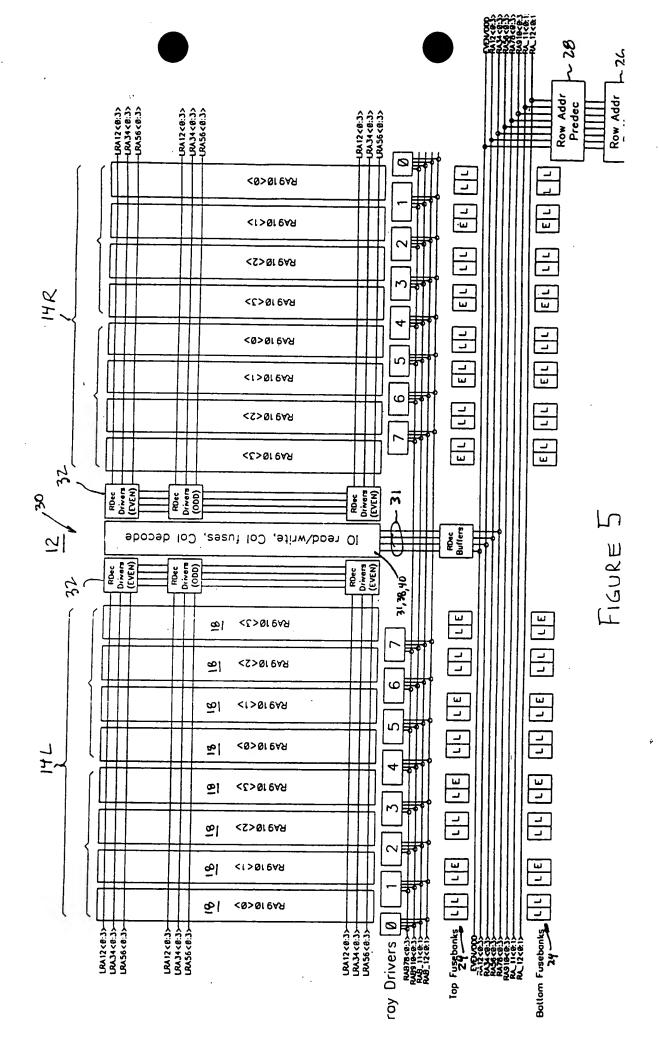


FIGURE 4



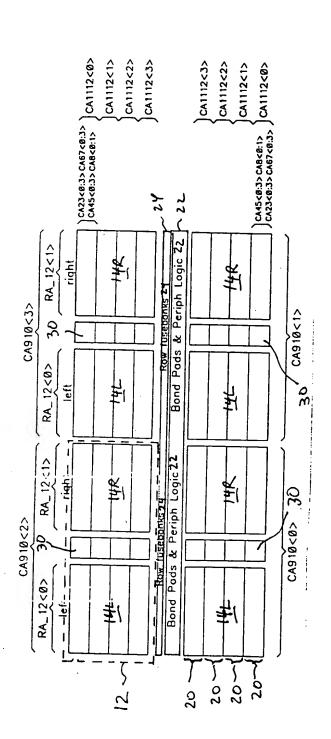
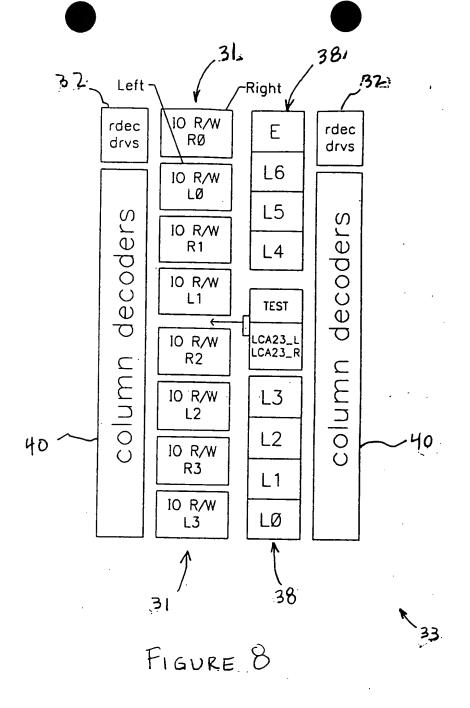


FIGURE 6

				88^	1						
	P.n. 28	× × ×	2 ×		X 16	8 8	X 4	ž		VCC Pin 2	
74 18 VSS VSS VSS	Pin 29 A6	88^		88 🗆 29	T-	 8	8^ -		<u> </u>	AS Pin 26	- CCCC - CCCC - CCCCC
\$CT_	Pin 38	554 554 5 5	. c'c.	33A 🖸 19 66 🖸 55A))	ACC .	۸۵۵	ΟOΛ		A4 Pin 25	
A6 A6 A6	AB 3	\$\$A \$\$A \$\$.	n SSA	8740 D 12	ON	224		οολ		₹ 2 2 2	<u> ১</u> ১১১
A7 A7	Pin 32	noise0 003 sol 0W		22 □ 02374 A190 □ 82	ON	ON	SOV	Σ		A2 %	P 44 4 5
والمالا	Pin 33 Pi	7A 7A 7/ 3A 3A 3/		\$Y \$\$	SA	\$4	۶A	ζA		1	[2]2]2] ²
AB AB 2		8A 8A 8/	-	** 15	• ₽∀	74	₽¥	Þ∀		2	S S S S
~	S	3, 3, 3,		(v □ 6»	ξA	ζA	£A	\$4		Ph 2	
A 89	A1235	6A 8A 6A	⁄ 6∀	8+ D 64	70	70	70	214		N 5	A2 A2 Pin 13
A 10 2	NC S6	01A 01A 014	/ 01A	\$> 0 700.00 \$> 0 81A \$A 0 7>	ZA	Σ∀	7∀	∀		NC Pin 59	1
<u> ইবিবার</u>	Pin 37	IIA IIA III	/ LLV	€+ □ 114	۲A	۱A	ſA	IA		NC is	444
A I I I	NC 38	SIA SIA SIA	, SIA	15 🗆 S1A	ØA	0¥	Ø۸	0 4		Si Si	2 8 8 8 E
	Pin 39 P	07C2 ——		18 □ ACCb 28 □ DACS			ove	_		NC Pin 56	§ 3
A A 12 25	e	or (CAS3) wc	- 24	16 □ cs22 CAS3 □ 37	274	> * ((CY25)	> *		NC S T	S S S S
କ୍ଷ୍ମି ଆଧାର				3 e 🖸 482	3w SA9	3W ZASI	3w	3w 8 4 5		1	• <u>ত্যিতাত্</u> য
S N N N	42 Pin 41 S UCAS	» 30 30	30	+5 🗆 30						RAS Pin 14	P RAS
2000	[일]	CAS (CAS CAS	∩C∀2	20 □ 12 20 □ 12 21 □ 12		•	(1 2 ‰)	> ~		Wind SI	«ريني»
e NO O	Pin 43 VSS	>* >* SS∧	SSA	31 ACCO 28 ACCO A220 33 A220 39	SOV	ΛCC	2/4	374		VCC Pin 12	W WE
CAS CAS CAS CAS CAS CAS CAS CAS CAS CAS	NC NC	>> >> S00	000 0010	35 🗆 800 75 🗀 800						NC Fi	VCC NC CS3)
돌이이이	25 mg			200 🗆 SZ	400 800		374 374	2% 2%		008 Pin 18	SIZIZI
NC NC VSS	Pin 46	>~ >~ 900 >~ >~ 900	0011	0016 🗆 23						007 Pin 9	N N N S
	Pin 47 Pi			\$1 () 002 \$6 () 004	900		>N >N	274 274		006 8 m	
N N N N N N N N N N N N N N N N N N N	Pin 48 Pin 10012 DG	<u> </u>	\dashv	000A 🗇 61	224		2%	2/4		_	S S S
N U U U		>+ 200 700 >+ >+ >+	SSA	81 0 055A						005 Pm 7	খ্রতাত :
* FIZIZI	et NSS	007 003 ↔	*100	91 🗆 C1000	200	200	DOS	> *		VCC Pin 6	S N N
NC N	Pin 58			NO □ 51	>* 003	005 ~		on NiQ		Pin 5	MC 222
	Pin 51	>> >00 800 >> >00 800		11 2100 \$1 4100	700	. 50	.00 .	000		003 Pin 4	
Pin 3	Pin 52 0015			900 6 900 6	100	100	100 1	noa		D02	SOS S
<u> ২</u> থিগৈথ	Pin 53	SSV SSV SSV SSV SSV SSV	SSA SSA	0000 0000 0000 0000 0000	ACC				0	00 ii	(JOJO) ~
VSS VSS VSS VSS	SSS F		ŀ	٠٠٠				·			
× × × - 4 8	· 12	1	91)	:	90	89 ;	* ×	į		9. ∑a	8 * ×

FIGURE 7



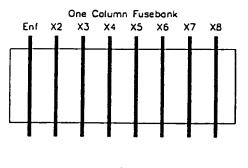


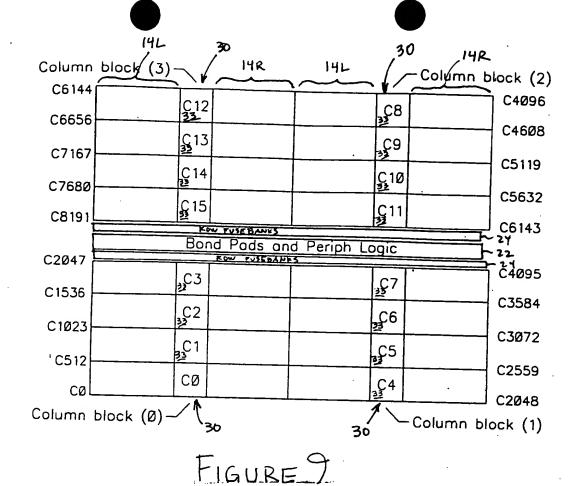
FIGURE 10

Row Redundant Laser Fuses

									4
	Row	Predec	Addr	BI	ow	Los	ser	Fuse	
	RA	12<0>		хØ		<u>a</u>	x2	[x3]	_
	RA	12<1>		ר	. –	_ ;	x2	[X3]	
	RA	12<2>		ר	· ~	ווי	<u>~~</u> x2	×3	
	RA	2<3>		ר	· 7=	록 ,	x2	x3	
	RA3	34<0>		ר	Ţ	า กั	×2	x3	
i	RAS	34<1>		ר	×	_ ;	×2	x3	
	RAS	34<2>		ר	×	—, ՟	×2	×3	
	RA3	34<3>		ר	×	= -	x2	x3	
1	RA5	6<0>		ר	×	กเ	×2]	x 3	
1	RA5	6<1>		ר	x '		*2		
	RA5	6<2>		ר	x 1		×2	<u>x3</u>	
	RA5	6<3>		ר	×	≒ ~	(2)	x3	
	RA7	8<Ø>		хØ	x 1		(2)	[x3]	
	RA7	8<1>		ר	×1	_ =			
	RA78	3<2>		ר	x 1		2	2	
ļ	RA78	3<3>		ר	×1	⊣	2	x3	
l	EVEN	ľ		xØ	x1	ן ה	2	×3	
	ODD			ר	x1	~ <u>=</u>	뒭	<u> </u>	1
		1<0>		ר.	x1] ×	_	x3	l
l	RA_1	1<1>		ר	x1	ĺ	2	x3	l
	RA91	0<0>		хØ	×1	[x:	_ ภ เ	x3	
	RA91	Ø<1>		ר	×1	x2	= :	x3	l
	RA9 1			ר	x1	×	_ :	x3	
_	RA9 1	0<3>		ר	×1	×2	2 '	x3	
	Note:	Boxed fu	ses or	e the	'blo	wn'	fuse	s.	

Pretest Address (compressed to 8meg block; unscrambled addresses)

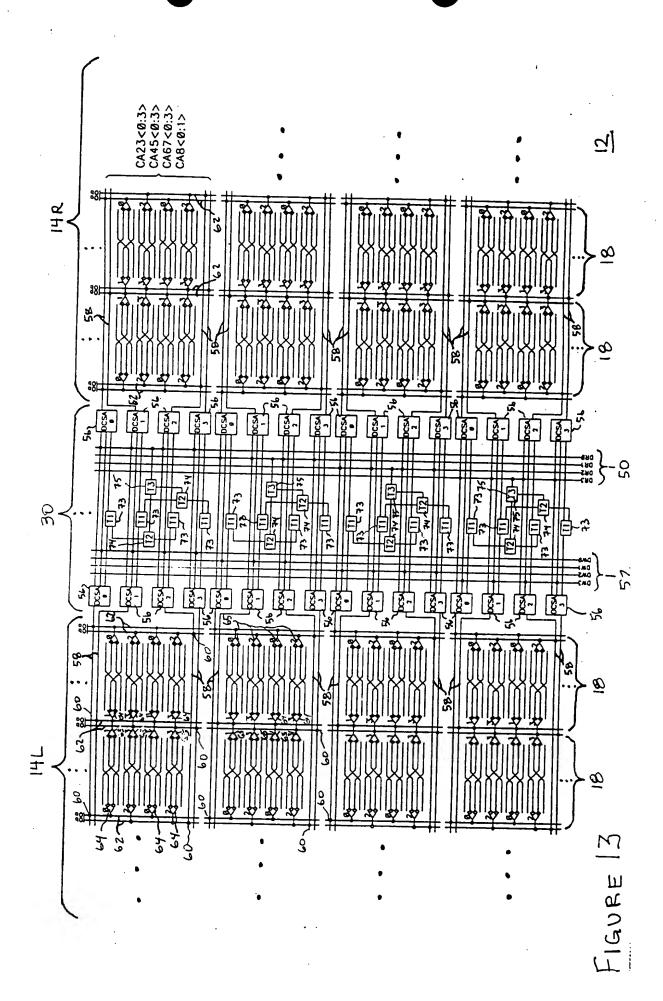
BLC	ОСК	ROW Addresses
RØ	R8	4,5,6,7
R1	R9	1016,1017,1018,1019
R2	R1Ø	1028,1029,1030,1031
R3	R11	2040,2041,2042,2043
R4	R12	2052,2053,2054,2055
R5	R13	3064,3065,3066,3067
R6	R14	3076,3077,3078,3079
R7	R15	4088,4089,4090,4091

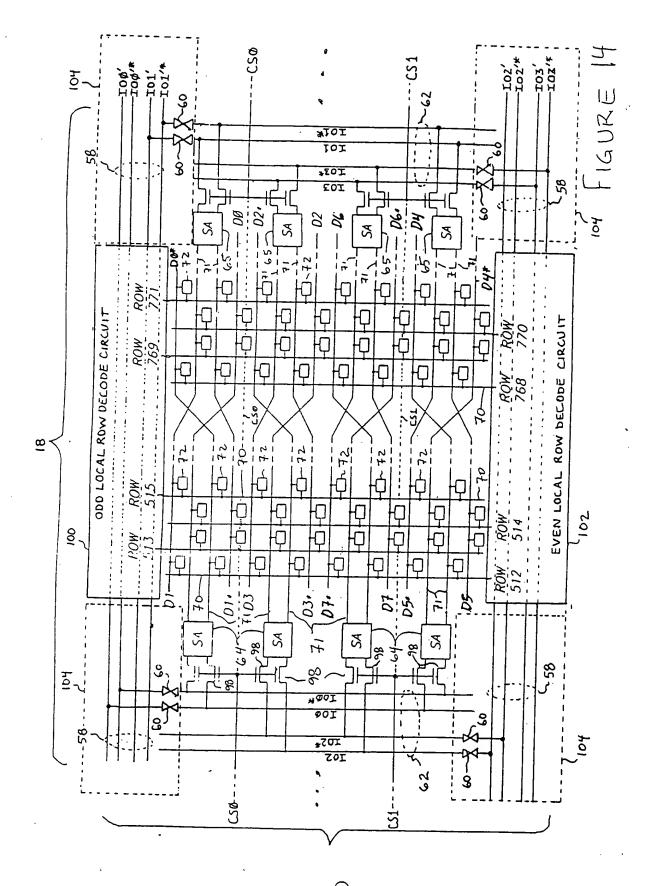


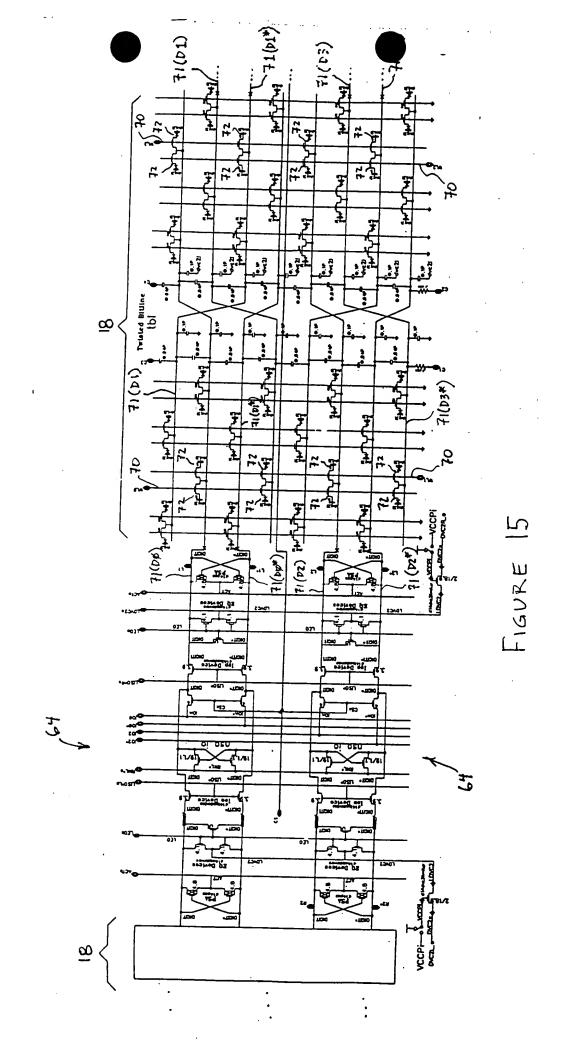
Column Redundant Laser Fuses

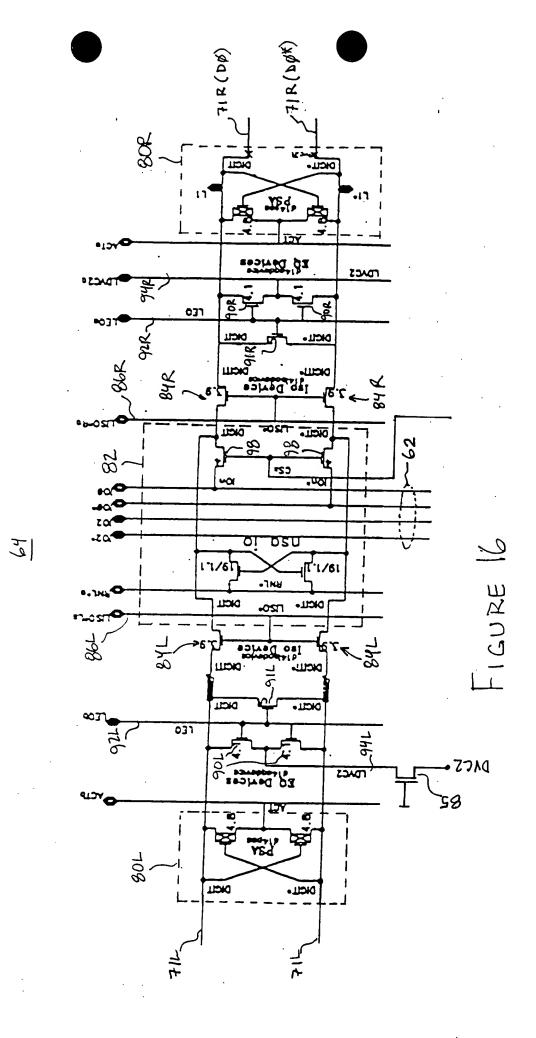
	Col Predec Addr	Blow Laser Fuse
	CA23<Ø> .	NONE
	CA23<1>	X2
1	CA23<2>	х3
	CA23<3>	X2, X3
	CA45<0>	NONE
1	CA45<1>	X4
	CA45<2>	X5
ĺ	CA45<3>	X4, X5
	CA67<Ø>	NONE
	CA67<1>	X6
l	CA67<2>	X7
	-eA67<3>	X6, X7
	CA8<Ø>	NONE .
	CA8<1>	X8

Bank	A8	A7	Pre-	-tes	t Ac	ddre A3	SS
Ø	Ø	Ø	Ø	Ø	1	· 1	1
1	0	ø	ø	ø	1	1	ø
2	Ø	Ø	Ø	Ø	1	ø	1
3	Ø	0	Ø	Ø	1	Ø	Ø
4	Ø	Ø	Ø	Ø	Ø	Ø	ø
5	Ø	Ø	Ø	Ø	Ø	ø	1
6	Ø	Ø	Ø	Ø	Ø	1	ø
				NA			_









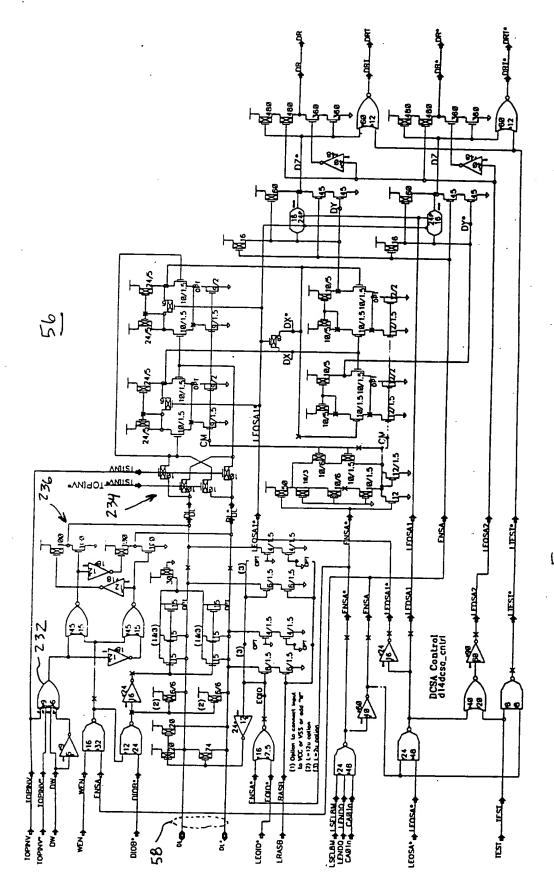


FIGURE 17

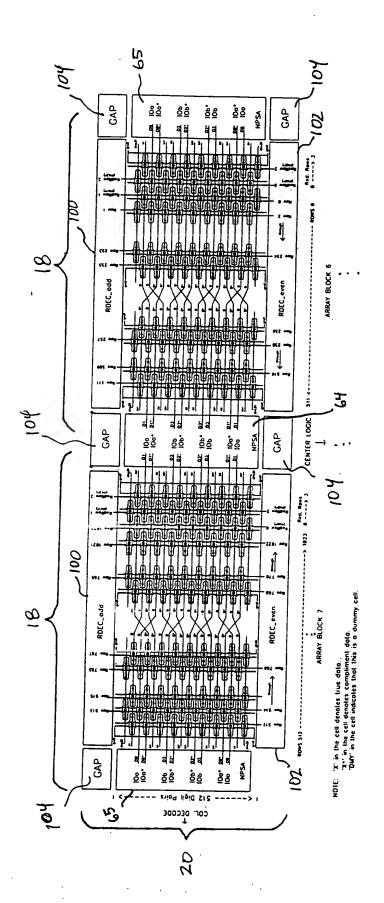


FIGURE 18

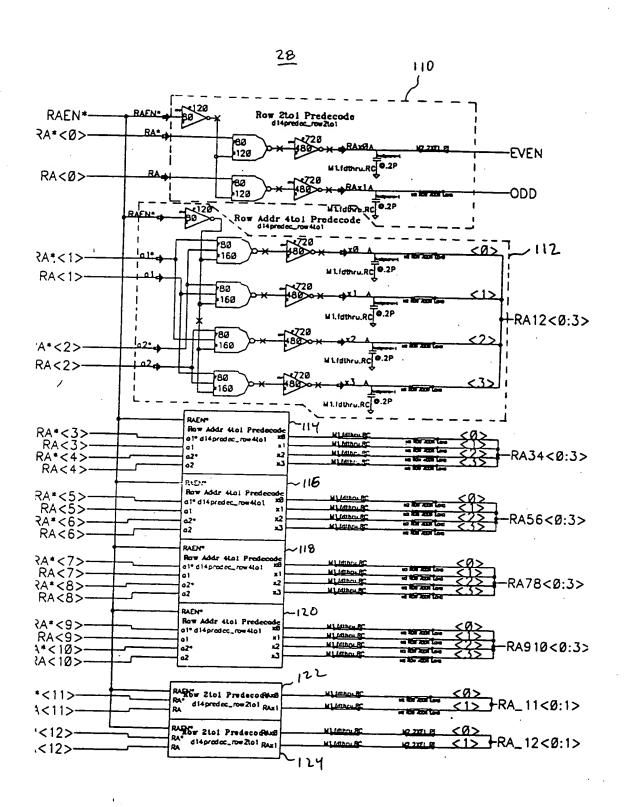
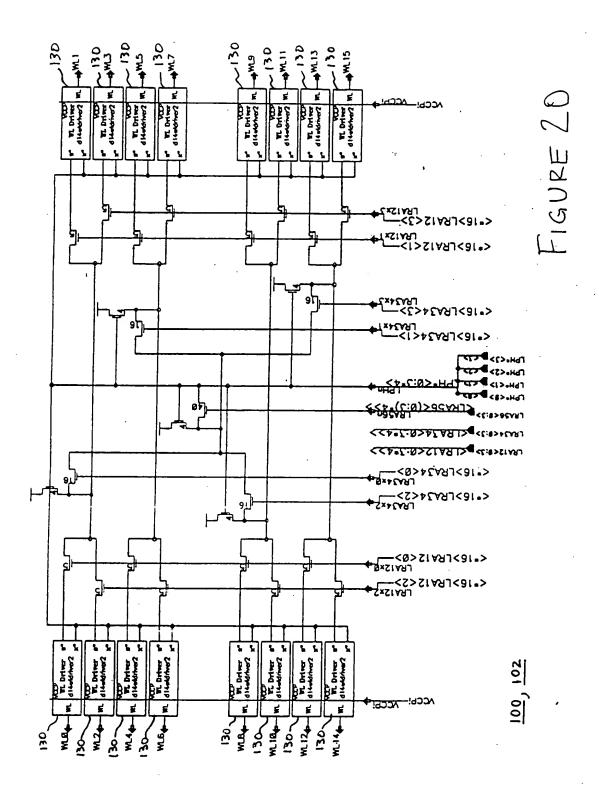


FIGURE 19



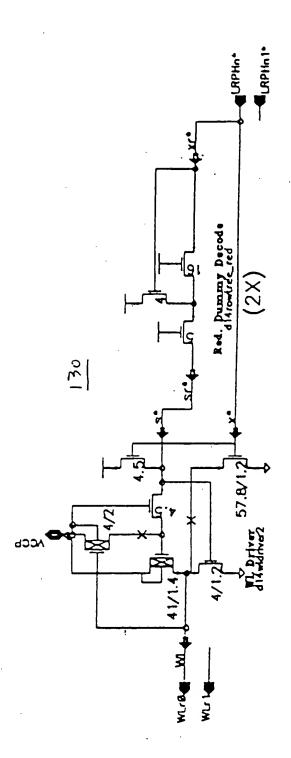


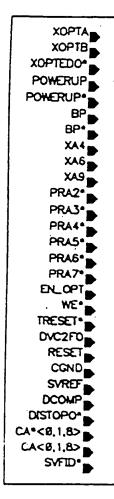
FIGURE 21

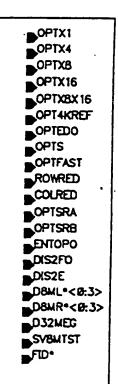
Laser/Electrical Fuse Options OPT4KREF COLRED not blown 8K Refresh (default) not blown fast EQIO/EQSA (default) 4K Refresh blown blown slow EQIO/EQSA **OPTFAST** not blown slow (default) OPTSRB OPTSRA blown fast Ref Rate not blown not blown 128ms (Default) **OPTS** blown not blown 192ms not blown fast-page (default) blown not blown 256ms blown static column blown blown 64ms ROWRED **ENTOPO** not blown not used not blown data topo on (default) not used blown blown data topo off

'	Bonding Options							
	XOPTA	хортв						
	NO	NO	OPTX16 (default)					
- 1	NO	VCC	OPTX8					
	VCC	NO	OPTX4					
- [VCC	vcc	OPTX1					
-	OPTEDO							
1	NO		no EDO (default)					
	VSS		EDO					

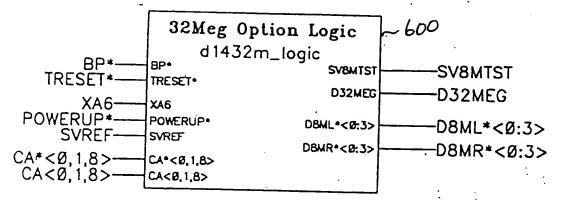
Oation Fund	Optio	n Add	ress			
Option Fuse	AIØ	A9	A8	A7	A6	A5
OPT4KREF	1	1	1	ø	Ø	ø
OPTS	1	1	1	6	ø	1
OPTFAST	1	1	1	0	1	0
ROWRED	1	i	1	ø	1	1
COLRED	1	1	1	1	ø	ø
OPTSRA	1	1	1	1	ø	1
OPTSRB	1	1	1	1	1	ø
ENTOPO	_ 1	1	1	1 -	1	1

INPUTS OUTPUTS





32MEG OPTION LOGIC



BONDING OPTIONS

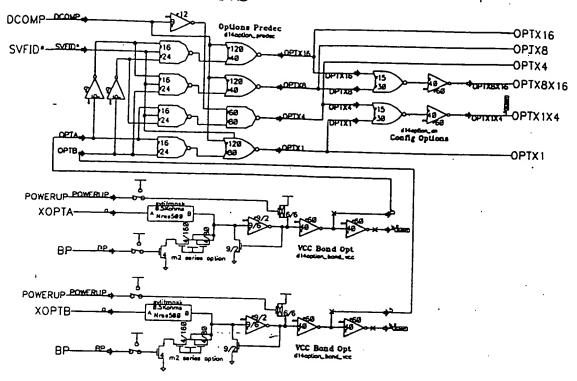


FIGURE 25

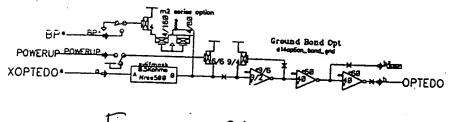


FIGURE 26

LASER FUSE I.D. ADDRESS

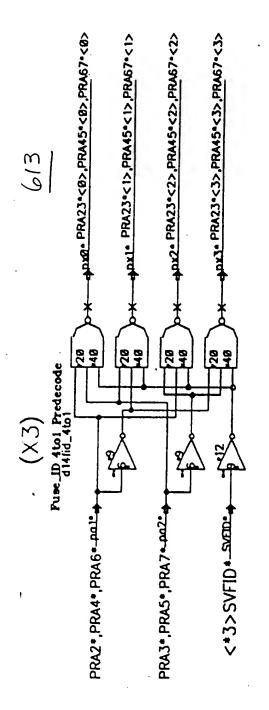
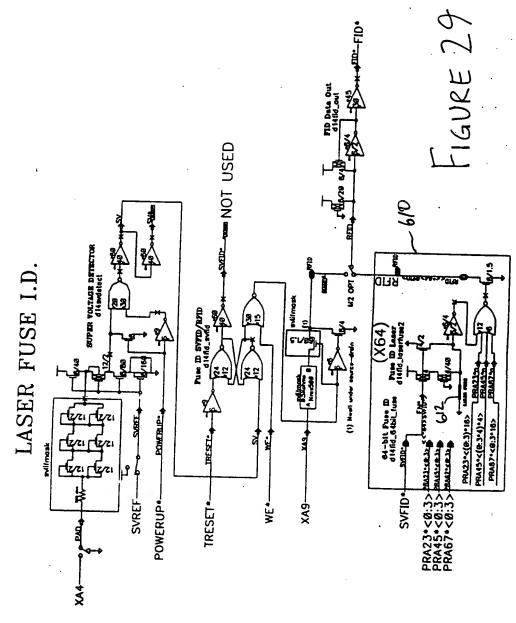
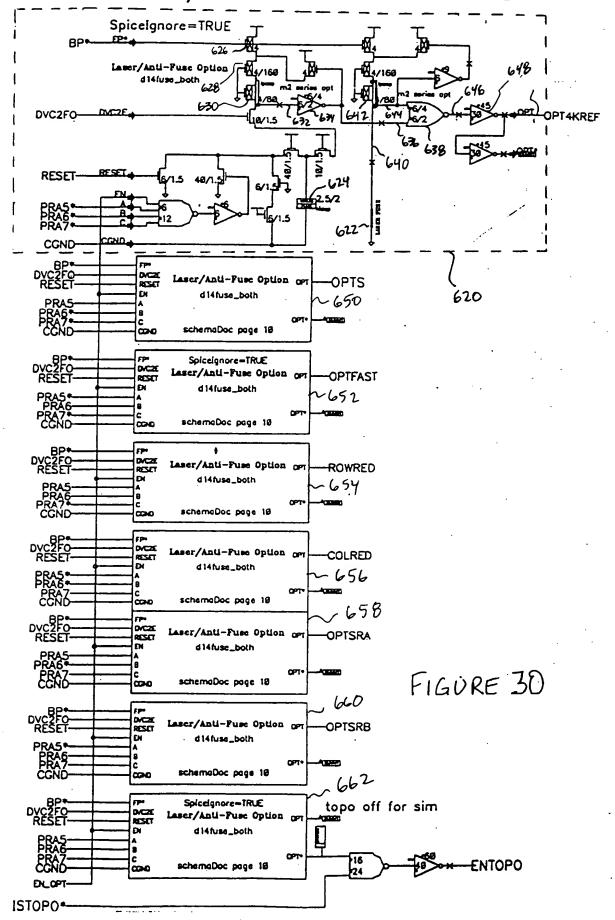


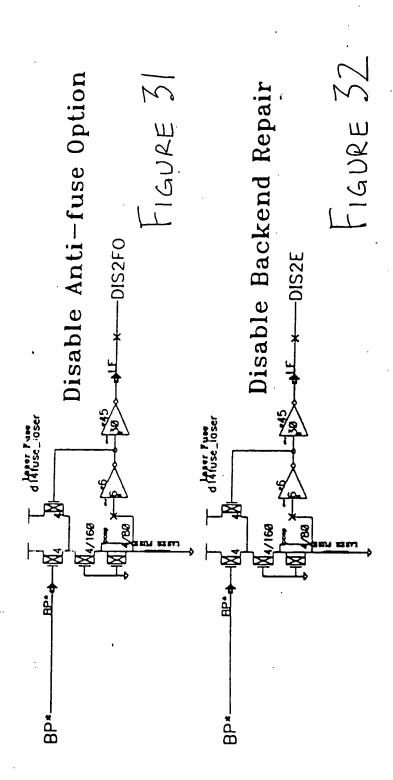
FIGURE 28



Fuse Blown = Logic "1"

LASER/ELECT FUSE OPTIONS





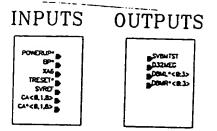
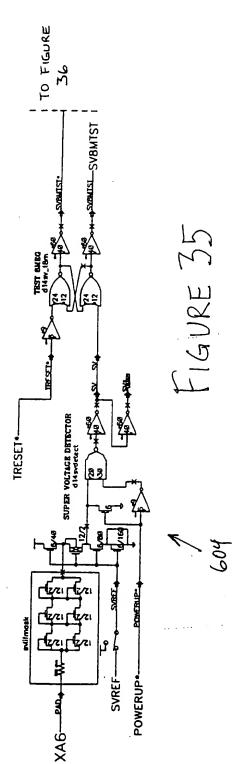


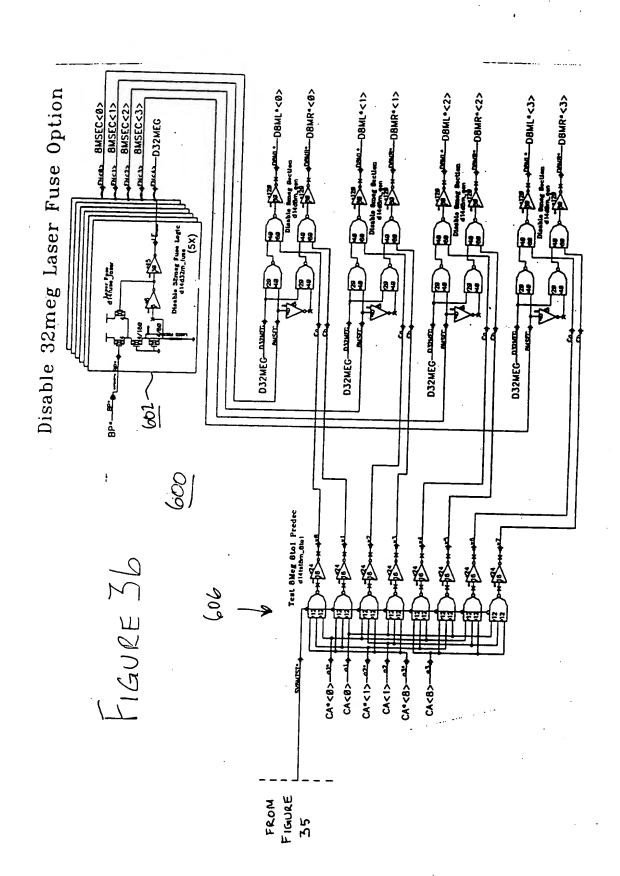
FIGURE 34

8Meg Arroy ICC-standby test

				· · · · · · · · · · · · · · · · · · ·	
/	A 1	A8	8 A7	Signal De-activated	Array Section Enabled (Ref to X4)
(0	Ø	Ø	D8ML*<Ø>	LEFT DQØ
(0	Ø	1	D8MR*<Ø>	RIGHT DQØ
(7	1	Ø	D8ML*<1>	LEFT DQ1
Q	0	1	1	D8MR*<1>	RIGHT DQ1
	1	Ø	Ø	D8ML*<2>	LEFT DQ2
	1	Ø	1	· D8MR*<2>	RIGHT DQ2
	1	1	Ø	D8ML*<3>	LEFT DQ3
1	1	1	1	D8MR*<3>	RIGHT DQ3

009 XA6 Supervoltage Detect/Latch





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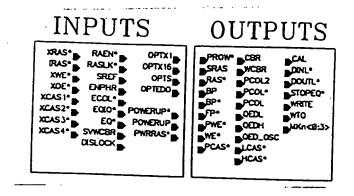


FIGURE 37

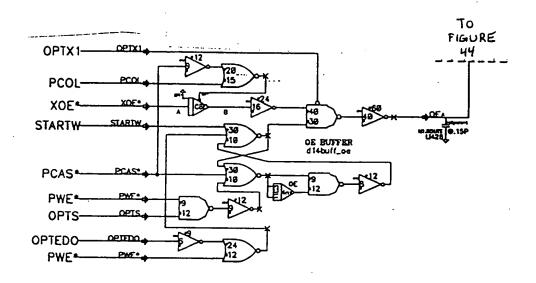


FIGURE 38

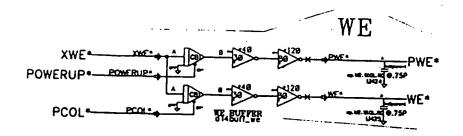
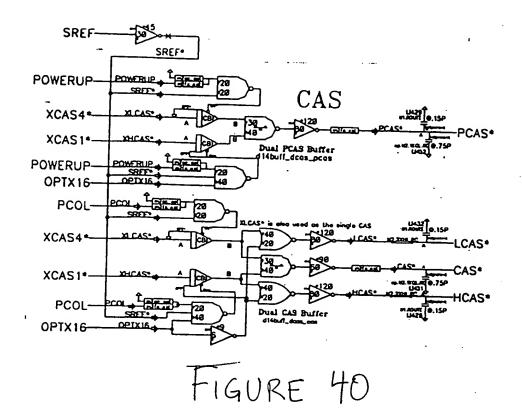
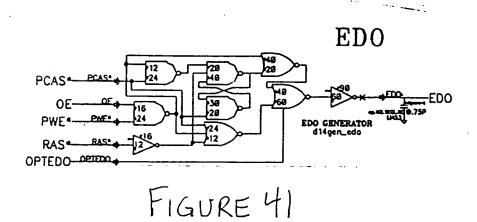


FIGURE 39





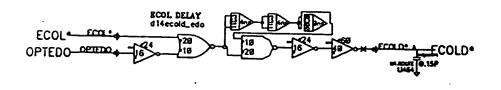


FIGURE 42

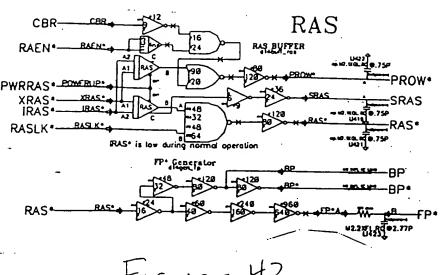
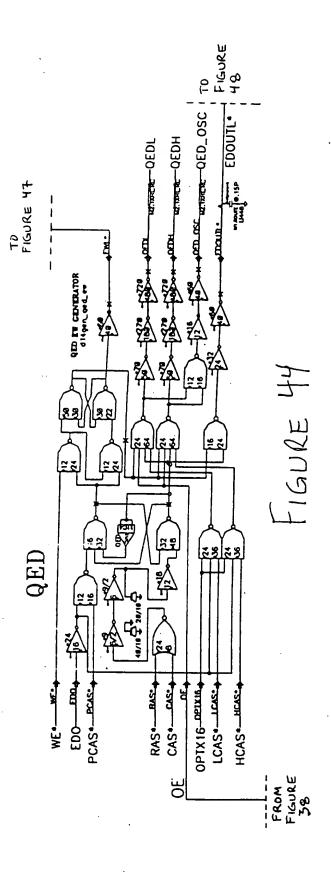


FIGURE 43



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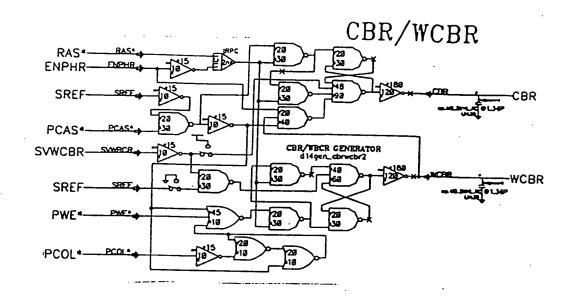
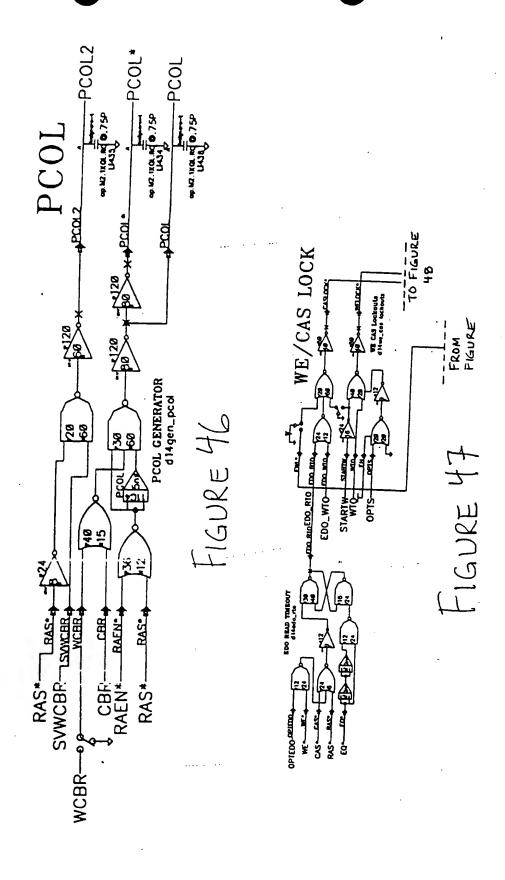


FIGURE 45



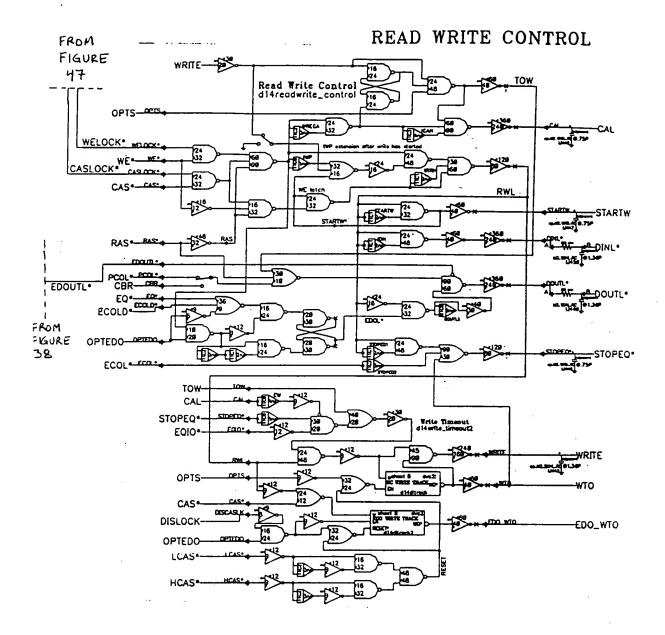
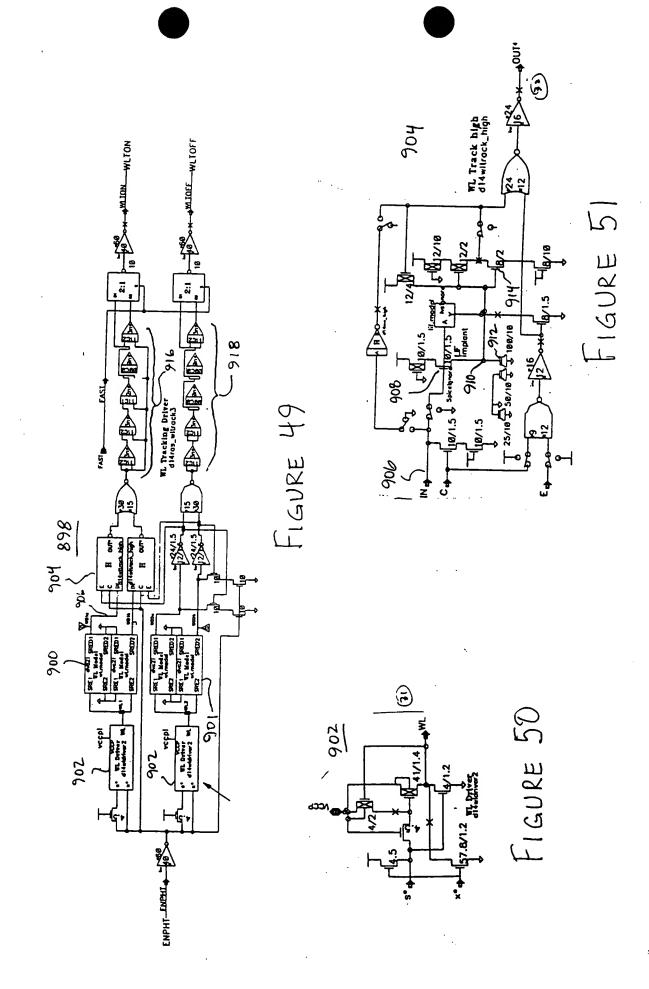


FIGURE 48



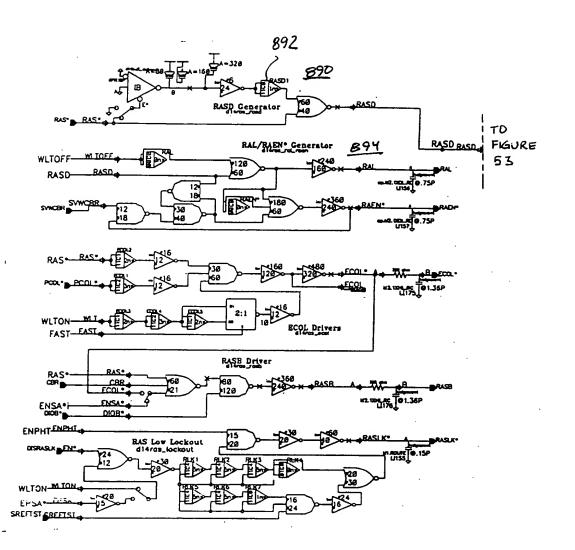
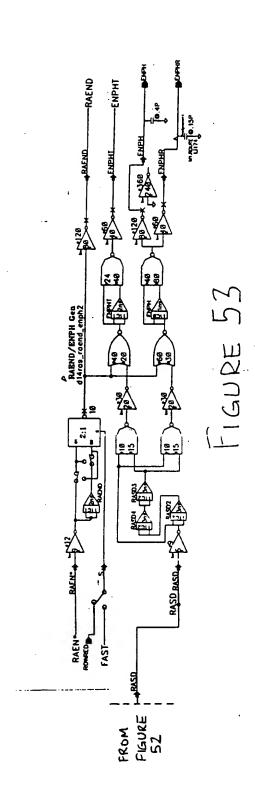


FIGURE 52



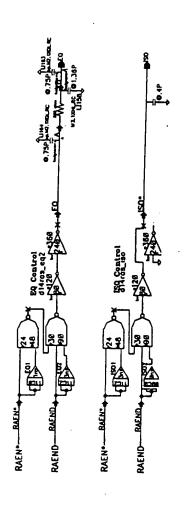
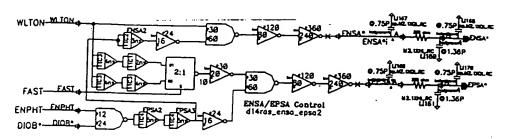
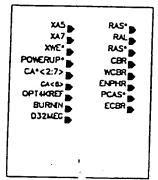


FIGURE 54

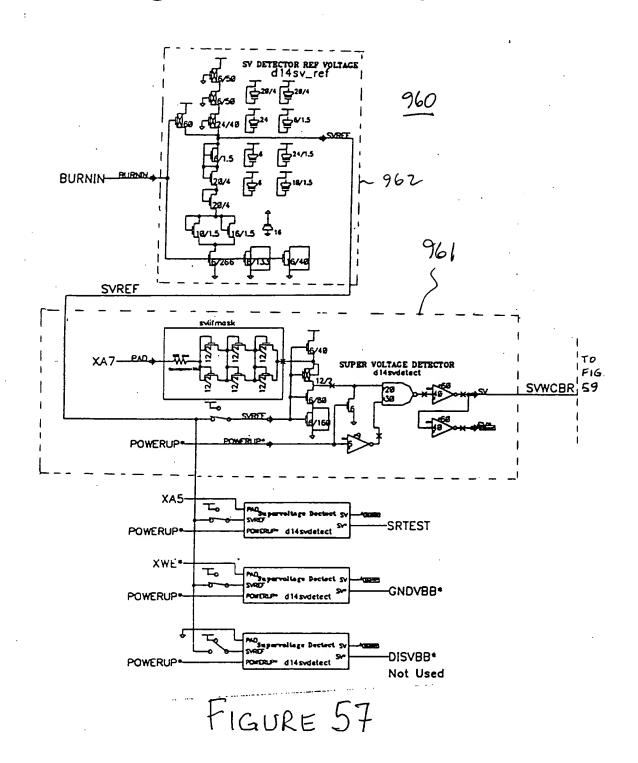


INPUTS



OUTPUTS

AFSTRESS DISTOPO- SREFTST



PROBE PAD

A Mone 548 8 Page 129 PAGE DIOB*

DIOB*

FIGURE 58

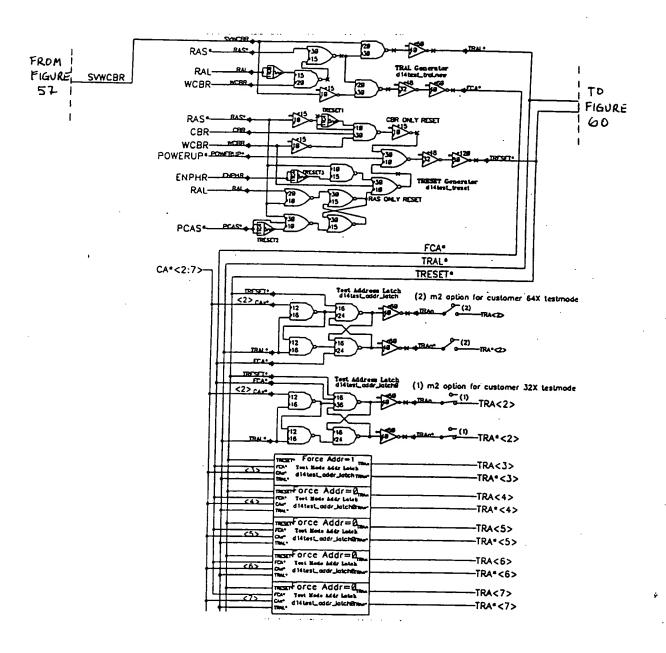


FIGURE 59

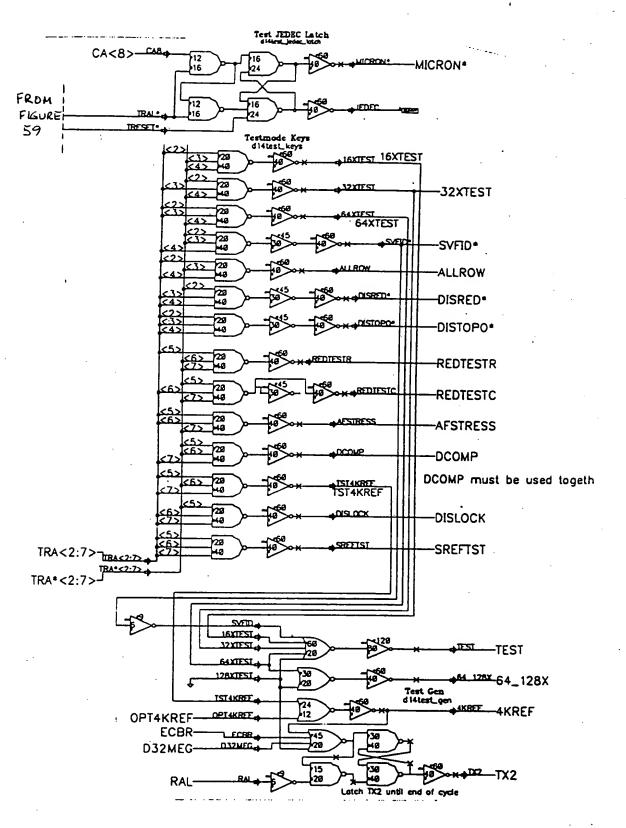


FIGURE 60

Test Mode Address Keys

A1 AØ A6 A5 A4 A3 A2	TEST MODE
0 0 0 1 0 1 0 1 1 1 1 0 1	no test 16X test 32X test 64X lest 64X lest Fuse I.D. Disable DVC2 w/ all rows high Disable redundant element Disable Data Topo no test Row redundant element pretest Column redundant element pretest Anti-fuse Stress test Test Data compression 4K refresh (otherwise 8K ref) Disable RAS/CAS lockout Self-refresh Test
0 1	JEDEC test mode MICRON test mode

FIGURE 61

Supervoltage and Backend Programing Inputs

Input Pad	Description of Usage	Page
<u> </u>		. age
AØ	generates PRGCANR)	8
. A1	generates PRGCANC	8.
A2	generates PRGR only if SVPRG is high	8
A3	generates PRGC	8
A4	supervoltage - Not Used	40
ļ A5	supervollage — self refresh test	7
A6	supervoltage — 8Meg ICC test	45
A7	supervoltage - WCBR	
A10	anti-fuse programming voltage	
All	supervoltage — elect fuse program SVPRG	8
WE	supervoltage — ground VBB	7
L		I

FIGURE 62

JEDEC/MICRON Testmode

READ	OUT	UTPUT		
DATA	JEDEC	MICRON		
All Ø's	1	Ø		
All 1's	1	1		
Different	Ø	Tristate		

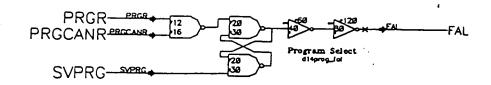


FIGURE 65

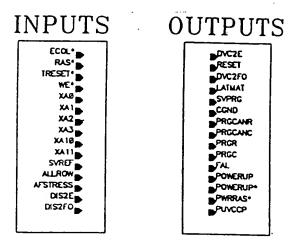


FIGURE 64

BACKEND REPAIR PROGRAMMING LOGIC

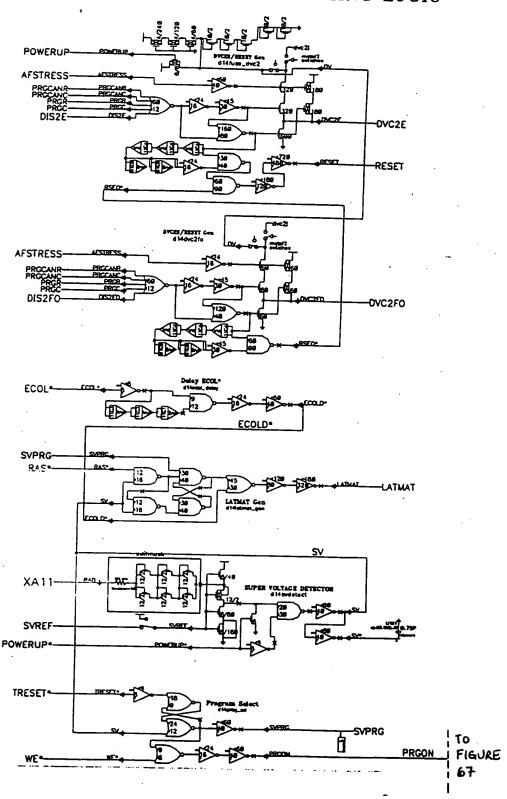


FIGURE 66

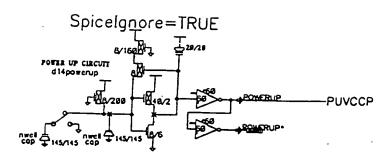


FIGURE 68

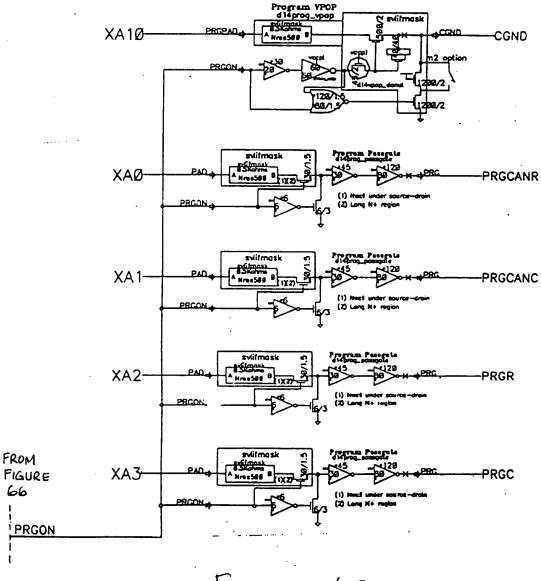


FIGURE 67

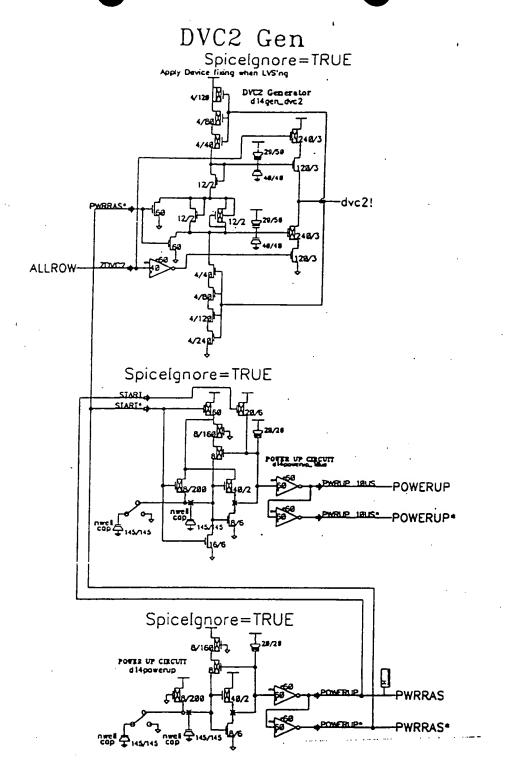
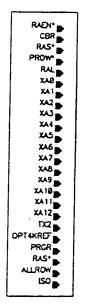
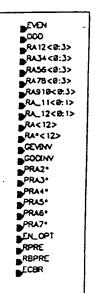


FIGURE 69

INPUTS OUTPUTS





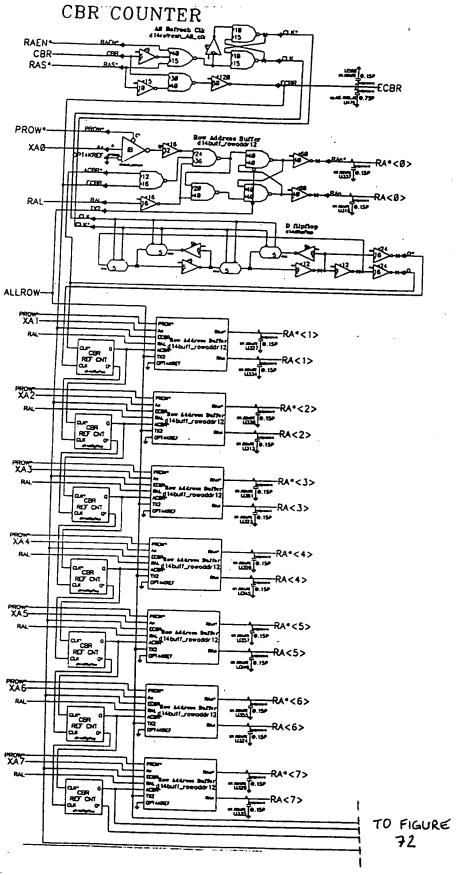
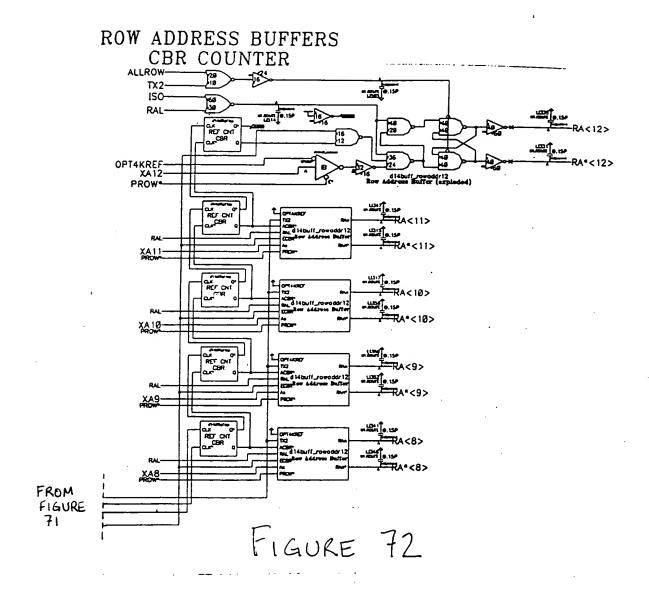
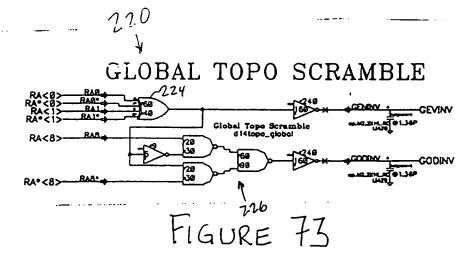


FIGURE 71





FUSE ID ADDRESS

FIGURE 74



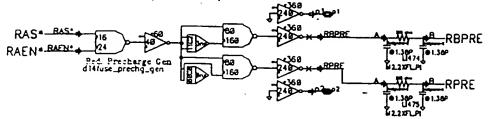


FIGURE 75

PORTION OF 25DE

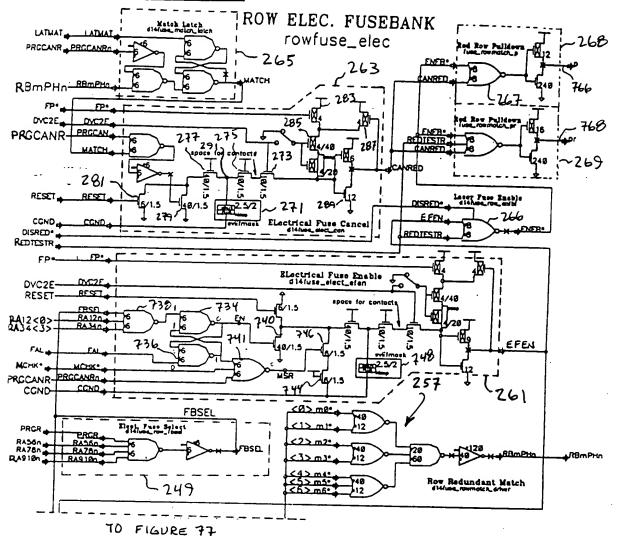
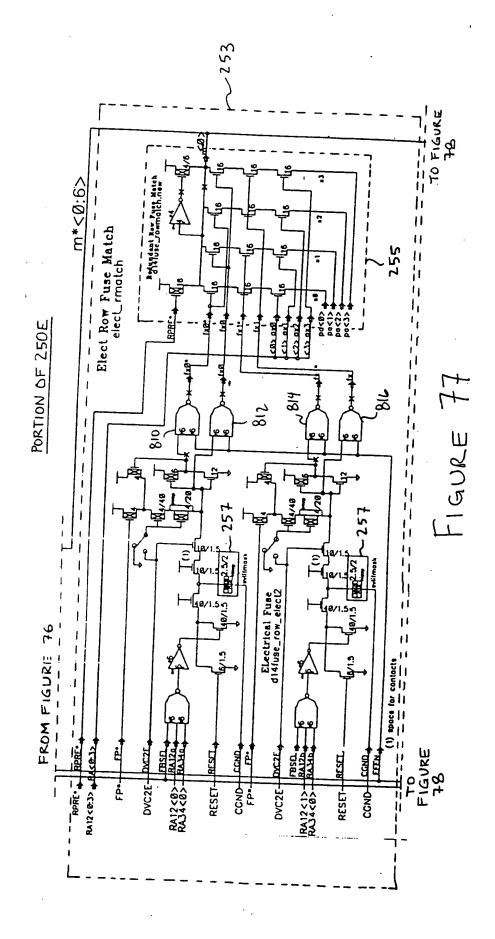


FIGURE 76



ROW LASER FUSEBANK rowfuse_loser MATCH PRGCANR-76² 50 CANRED 760 270 m*<0:6> 274 270 pb<83 pb<13 pb<23 pb<33 RPRE4-274 270 277 270 pd<8: pd<1: pd<2: pd<3: 274 270 274 FIGURE 79 274

250L

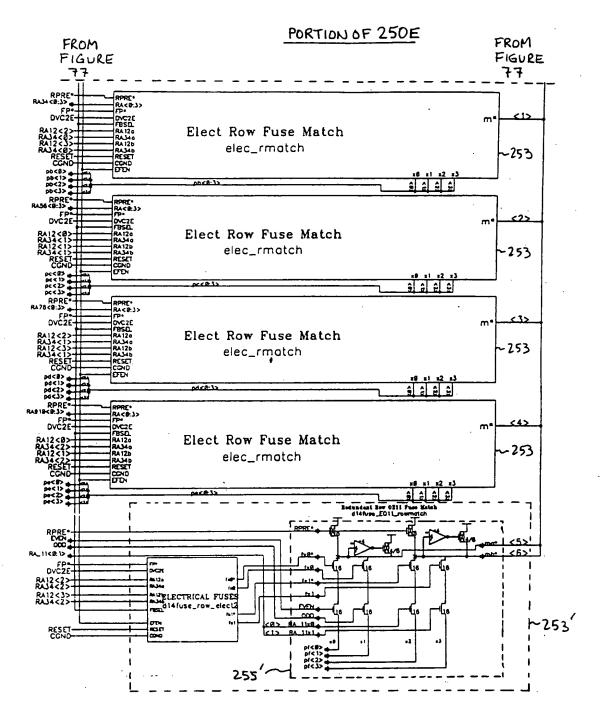


FIGURE 78

INPUTS

RPRE*_L_
RPRE*_R
RA 12 < 0:3>
RA34<0:3>
RA56<0:3>
RA78<0:3>
RA910<0:3>
RA_11<0:1>
EVEN
ODD
RA910n

OUTPUTS

```
RB8PH_B<8:3>
RB1PH_B<8:3>
RB1PH_T<8:3>
RB1PH_T<8:3>
RB2PH_B<8:3>
RB2PH_T<8:3>
RB3PH_B<8:3>
RB3PH_T<8:3>
RB4PH_T<8:3>
RB4PH_T<8:3>
RB5PH_B<8:3>
RB5PH_B<8:3>
RB5PH_T<8:3>
RB6PH_T<8:3>
RB6PH_T<8:3>
RB7PH_B<8:3>
RB7PH_T<8:3>
RB7PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR87PH_T<8:3>
RR8918_L<8:3>
RR8918_L<8:3>
RR8918_L<8:3>
RR8918_L<8:3>
```

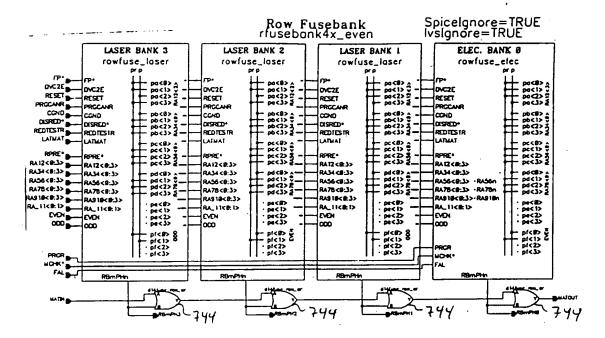


FIGURE 81

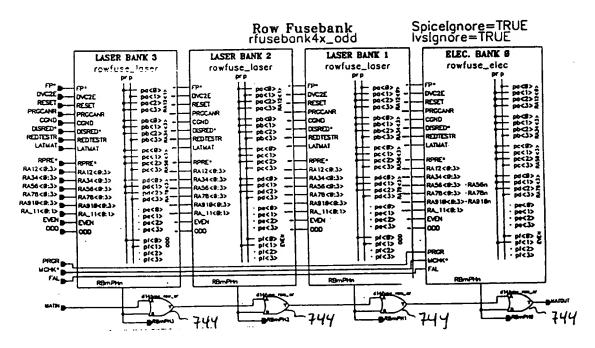


FIGURE 82

FIGURE 83

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	FP— PRCANTI— CCNNT— CCNNT— CCNNT— CONTEXP— REDIESTR— REDIESTR— RAIZ- RAI	RA, 11(8):15- EVEN- EVEN- PRCR- MCHK_1* FAL-	MCHK 8° FAL— PRGR— 000— EVEN RA, 11(8:1)— RA918(8:3)— RA36(8:3)— RA36(8:3)— RA36(8:3)— RA36(8:3)— RA36(8:3)— RA36(8:3)—	LATALATA LATALATA REDIESTR— USAGO- PRCCANTB— PREST— PREST— FP- FP-
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FIGURE 84

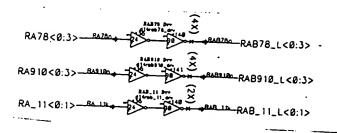
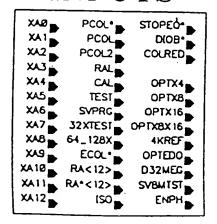


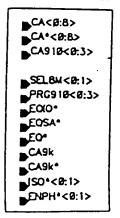
FIGURE 85

RA78<0:3>
RA78<0:3>
RA78<0:3>
RA910<0:3>
RA910<0:3>
RA910
RA

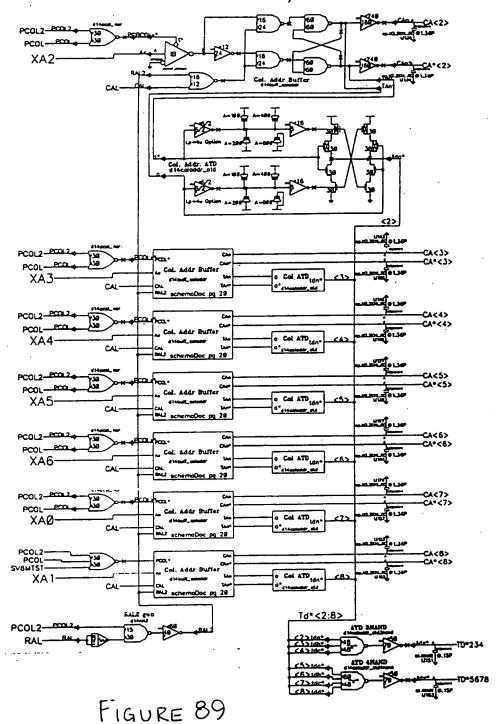
INPUTS



OUTPUTS



COLUMN ADDRESS BUFFERS/ATD



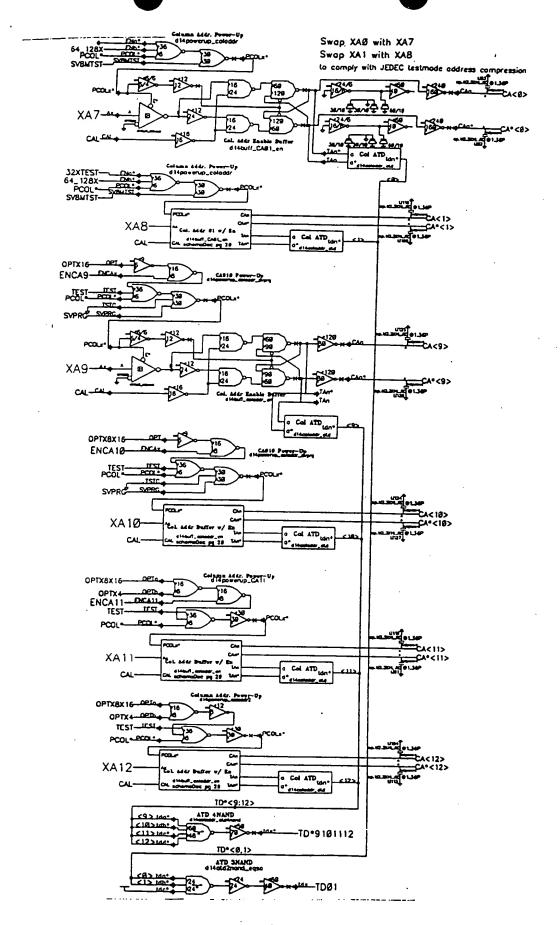


FIGURE 90

CONFIC	ROW ADDRESS	DRESS	COLUMN	COLUMN ADDRESS
	8K ref	4K ref	8K ref	4K ref
4MX16	AØ - A12	AB - A11	AQ - A8	AØ - A9
8MX8	AB - A12	AB - A11	AB - A9	AB - A18
16MX4	AØ - A12	AB - A11	AB - A1B	AB - A11
64MX1	AØ - A12	ı	AB - A12	I

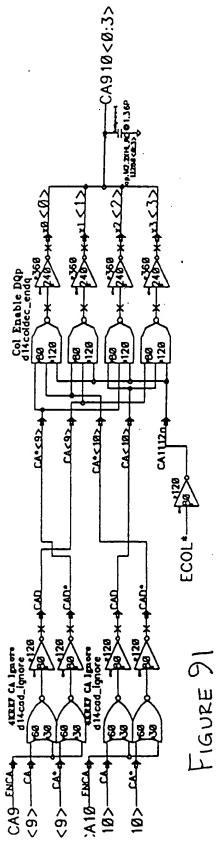
er to X1) e ignored			, A7	. A7. RA12	
rest mode Address Compression (rei to X1) The following column oddresses are ignored	A12, A11, A10, A9	A12, A11, A10, A9, A8	A12, A11, A10, A9, A8,	A12, A11, A10, A9, A8, A7, RA12	
The follow	16X	32X	64X	128X	

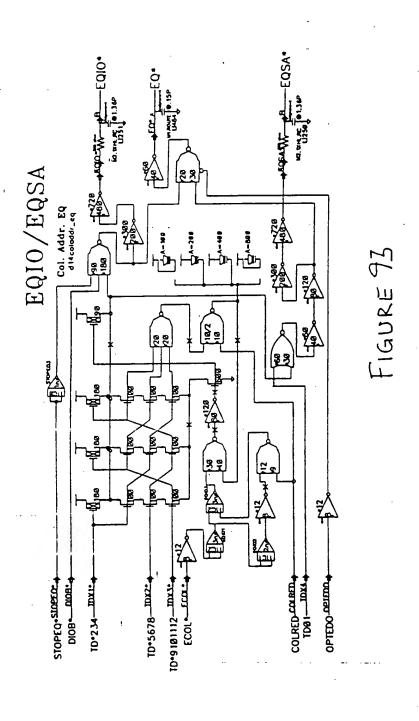
27.28

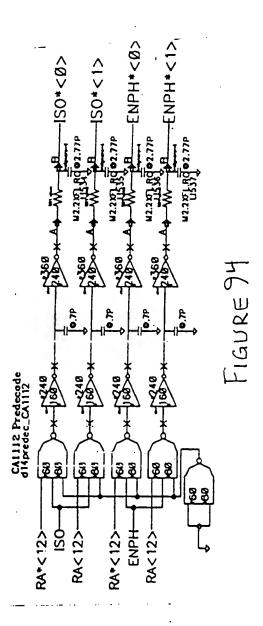
SPARE - 128

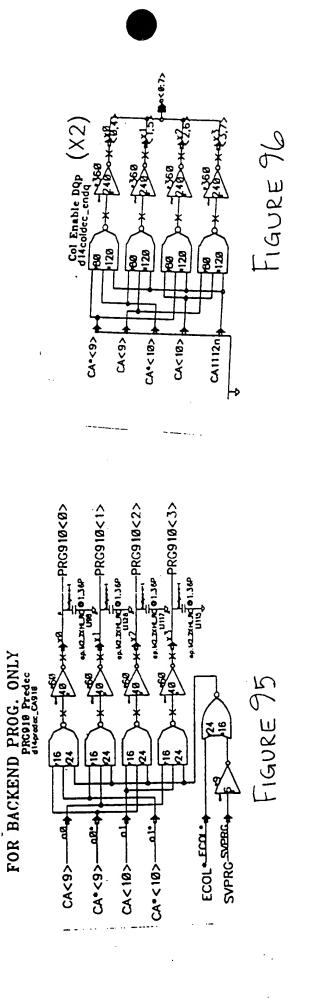
FIGURE 88

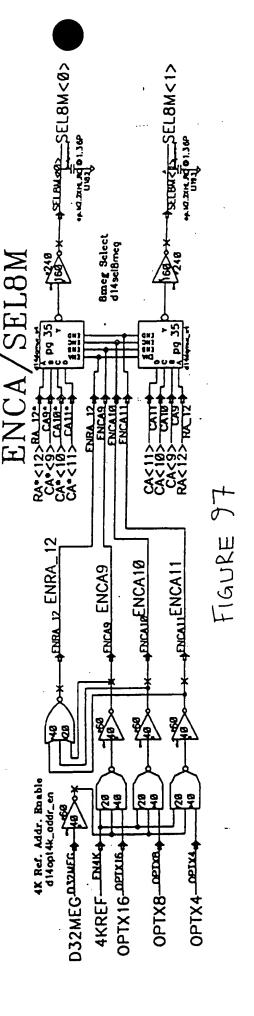


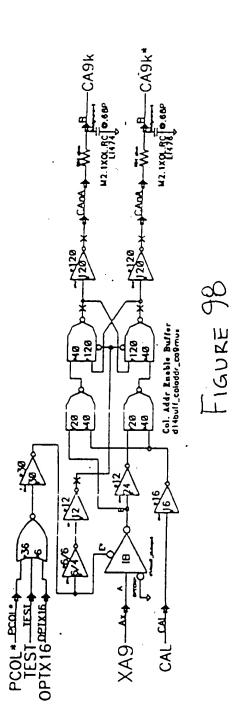












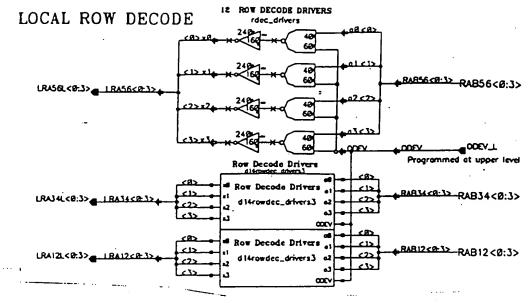


FIGURE 99

COLUMN SELECT

COLUMN DECODE CS<8-127>

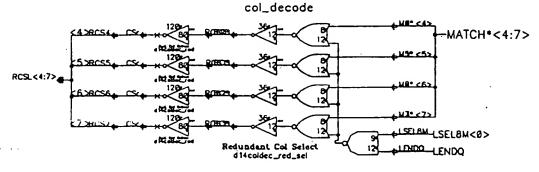


FIGURE 100

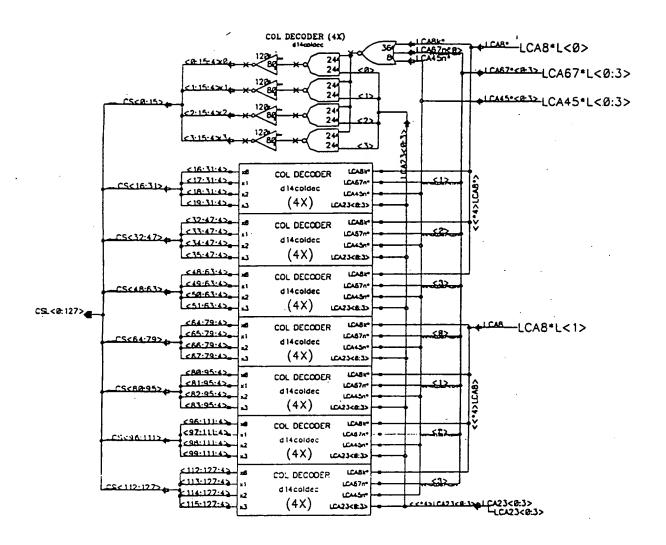


FIGURE 101

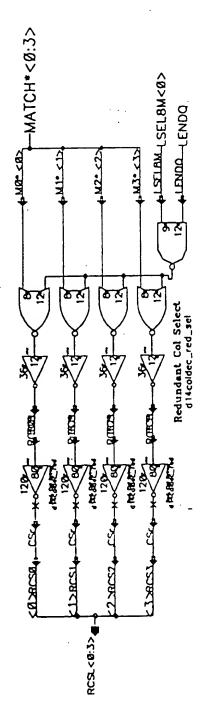
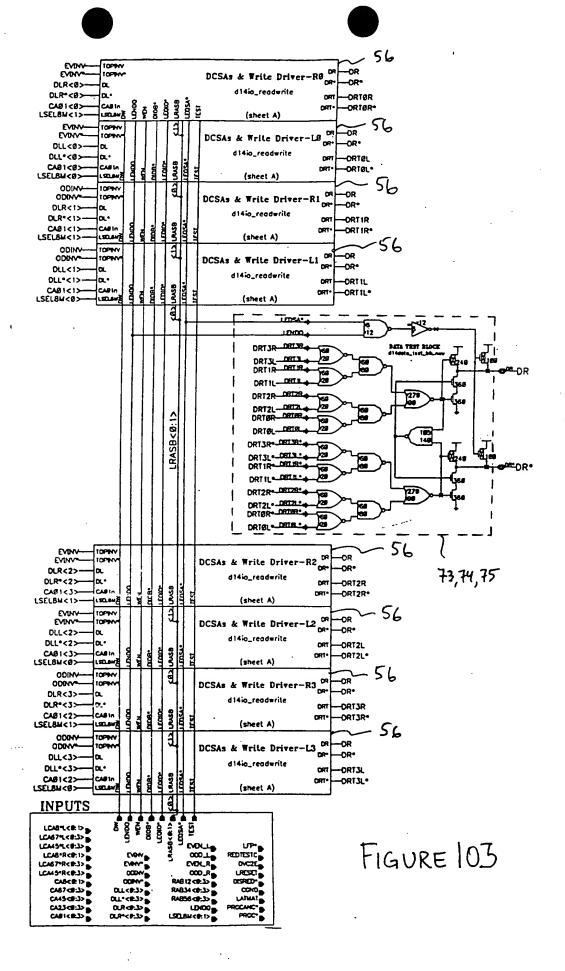
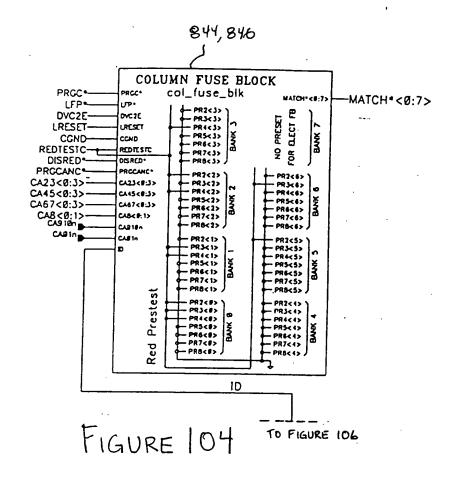


FIGURE 102





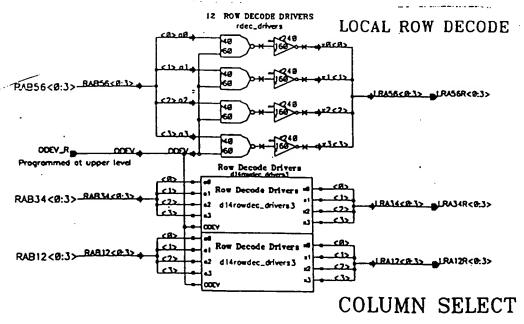


FIGURE 105

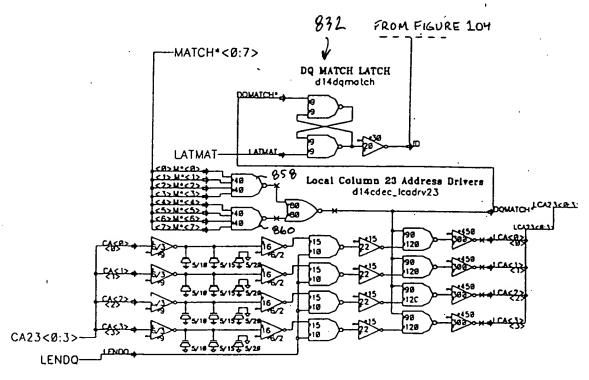


FIGURE 106

COLUMN DECODE CS<0-127>

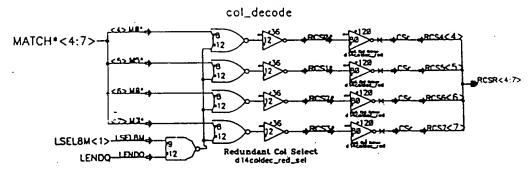


FIGURE 107

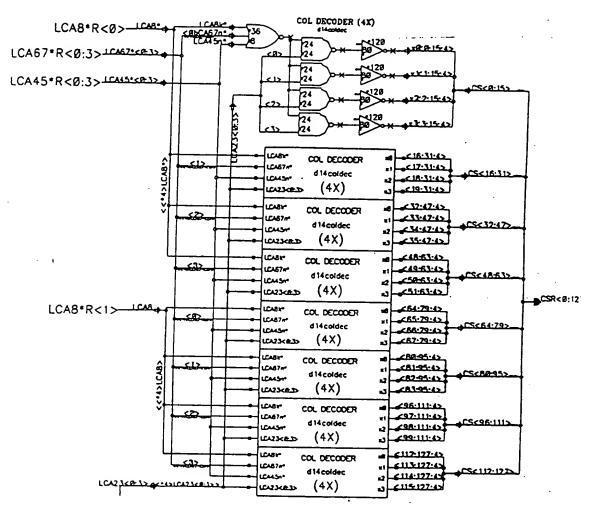


FIGURE 108

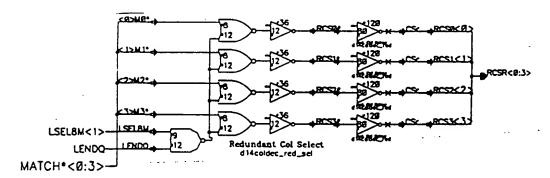


FIGURE 109

SEVEN LASER FUSE BANKS

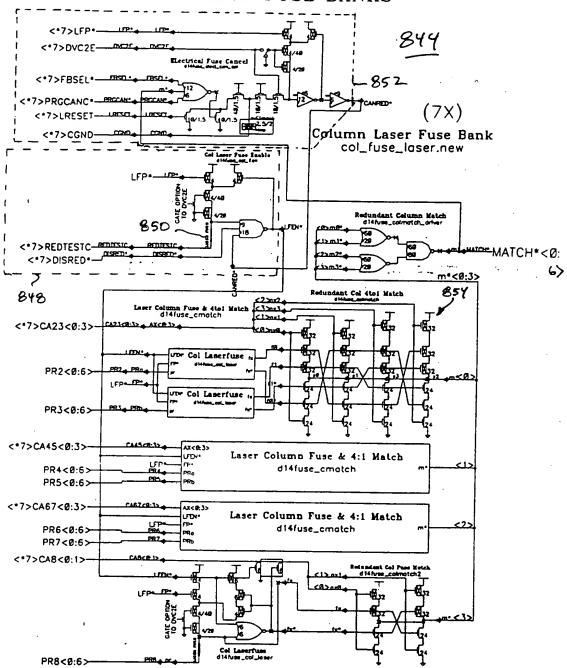


FIGURE 110

INPUTS

CA23<0:3>	PR2<8>	PR2<2>_	PR2<4>	PR2<6>
CA45<0:3>	PR3<0>	PR3<2>	PR3<4>	PR3<6>
CA67<0:3>	PR4<0>	PR4<2>	PR4<4>	PR4<6>
CA8<0:15	PR5<0>	PR5<2>	PR5<4>	PR5<6>
CAØ In	PR6<0>	PR6<2>	PR6<4>	PR6<6>
CA9181	PR7<Ø>	PR7<2>	PR7<4>	PR7<6>
UP.	PR8<0>	PR6<2>	PR8<4>	PR8<6>
DVC3E	-	_		_
URESET	PR2<1>=	PR2<3>=	PR2<5>	
CCMD	PR3<1>	PR3<3>	PR3<5>	
REDTESTC	PR4<1>	PR4<3>	PR4<5>	
O(285D).	PR5<1>	PR5<3>	PR5<5>	
PRGCANC*	PR6< 1>	PR6<3>	PR6<5>	
PRGC ·	PR7<1>	PR7<3>	PR7<5>	
10 <u> </u>	PR8< 1>	PR8<3>	PR8<5>	

FIGURE 111

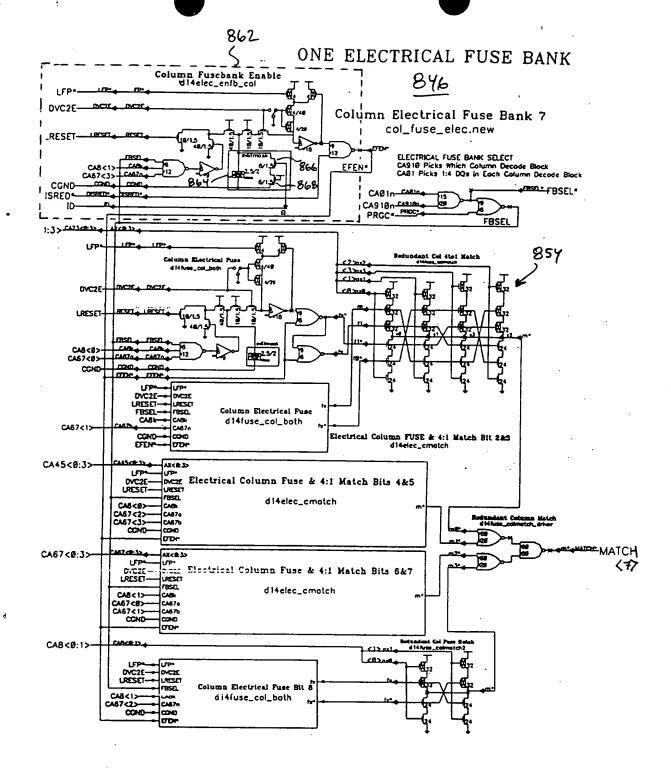


FIGURE 112

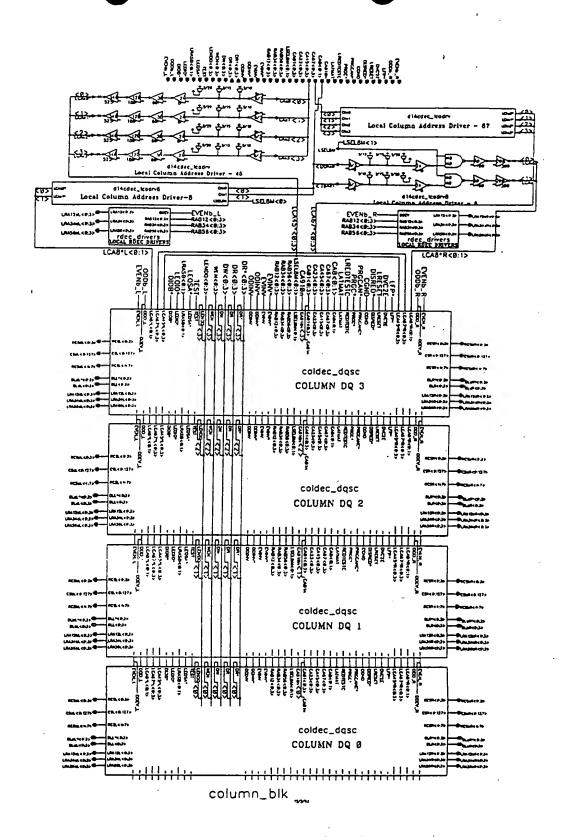


FIGURE 113

INPUTS FROM PERIPH.

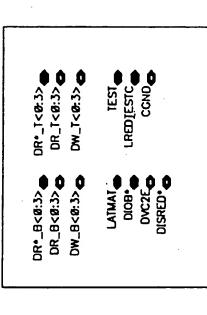
FASB EGSA EGIO GEVINV GODINV FP PRCCANC PRCC RESET ENTOPO	
EVEN DOD PRA12<8:3> PRA34<8:3> PRA34<8:3> PRA56<8:3> PRA-12<8:1> PRC918_B PRC918_B PRC918_B PRC918_B PRC918_B PRC918_F P)
CA<0:8> CA*<0:8> CA9:8> CA9:8> ECOL* MKn<0:3> LCAS* HCAS* WRITE CA9 10_B CA9 10_B CA9 10_B DBML*_B)

OUTPUTS TO COLUMN BLOCK

ODDb_LT EVENb_LT ODDb_RT EVENb_RT LEGIO* CA01<0:3> CA23<0:3> CA45<0:3> CA45<0:3> CA45<0:3> CA67<0:3>
COODD_LB CVEND_LB COODD_RB EVEND_RB RAB 12 < 0:3> RAB 34 < 0:3> LFP LFP LRESET PRGCANC
ODINV_T EVINV_T ODINV*_I EVINV*_I WEN_T<8:3> 'ENDO_T<8:3> LCA910_T LSELBMT<8:1> RAB_12T<8:1> LRASBT<8:1>
ODINV_B EVINV_B ODINV"_B EVINV*_B WEN_B<0:3> LCA910_B LCA910_B LSELBMB<0:1> RAB_128<0:1> LRASBB<0:1>

FIGURE 115

FIGURE 114 SIGNALS PASSING THROUGH



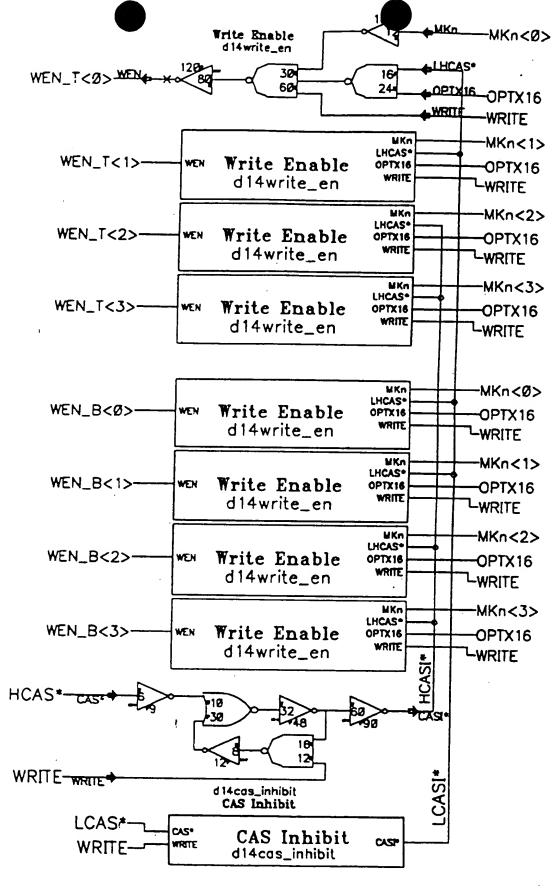


FIGURE 117

INPUTS FROM BOTTOM ROW RED.

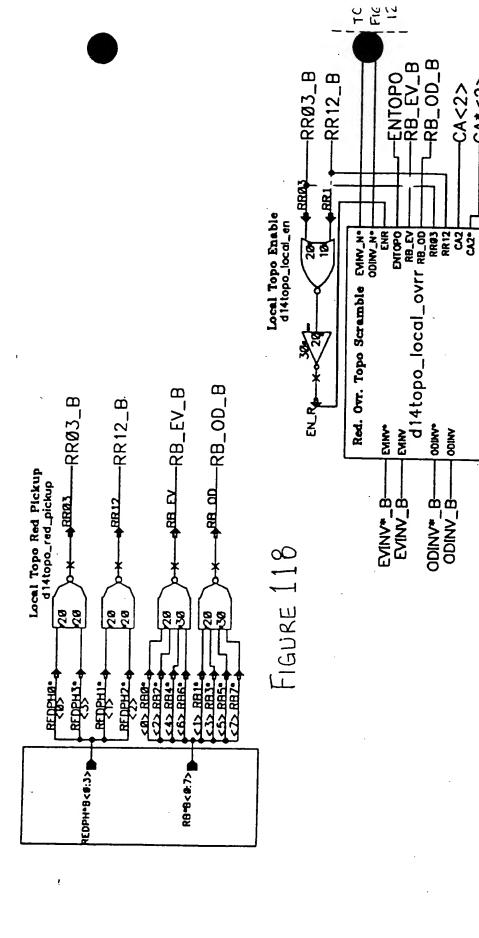
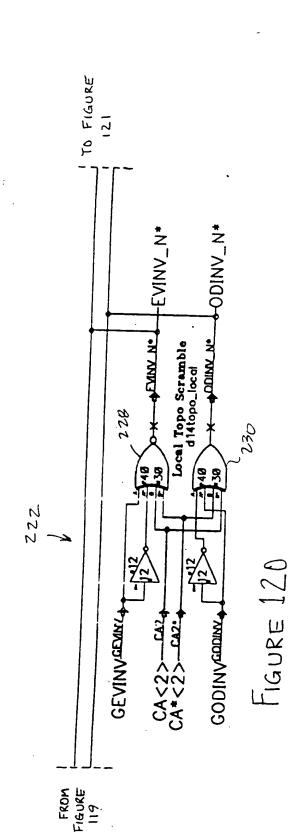


FIGURE 119

-CA<2>



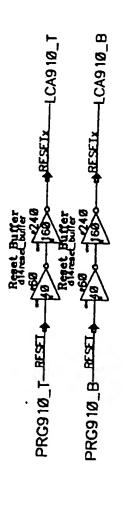


FIGURE 122

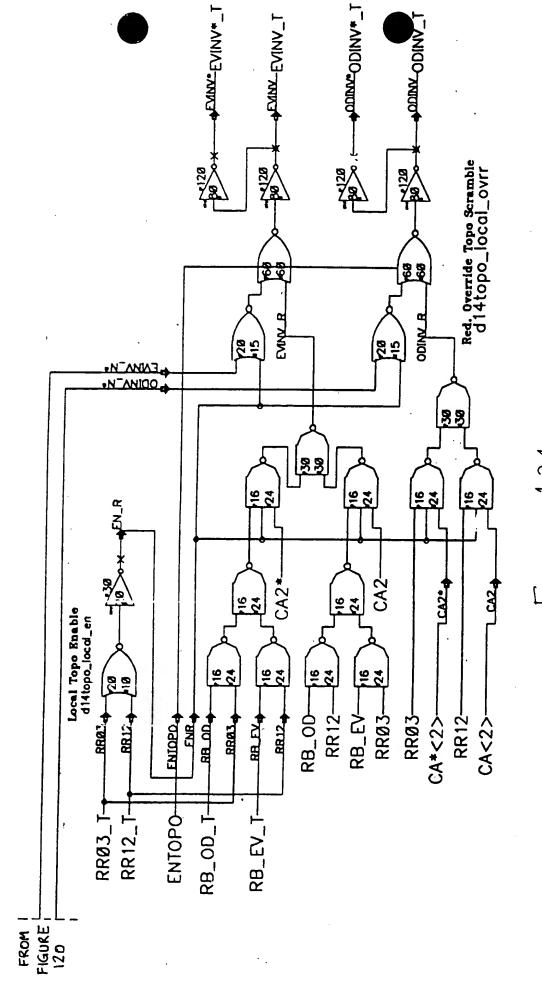


FIGURE 121

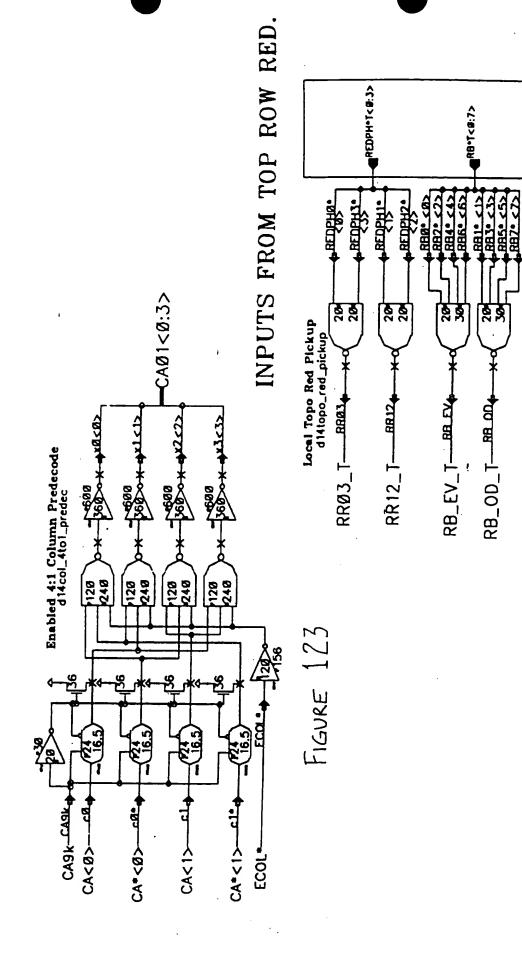
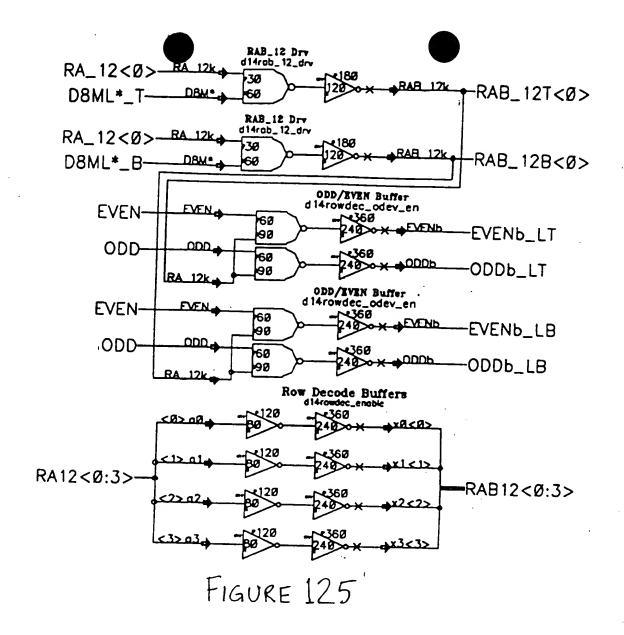
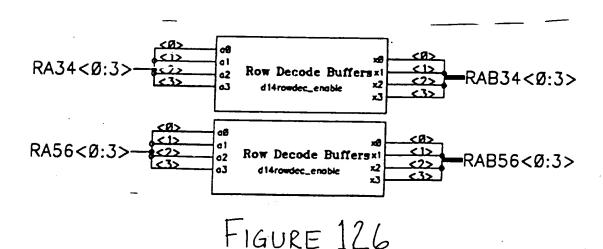


FIGURE 124





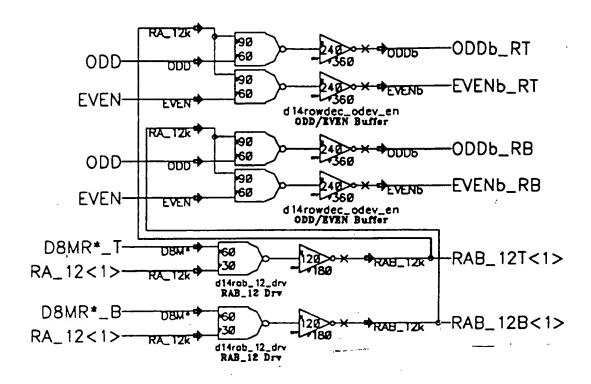


FIGURE 127

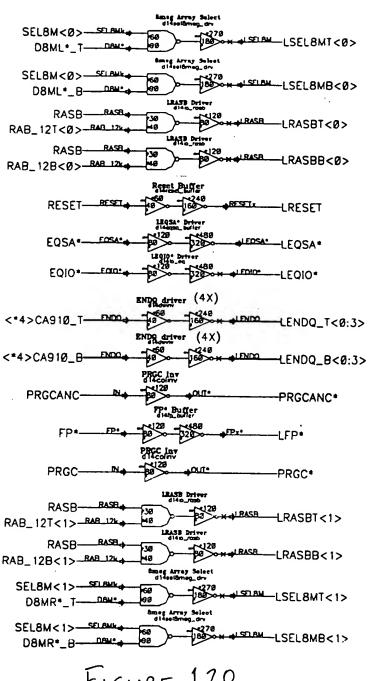


FIGURE 128

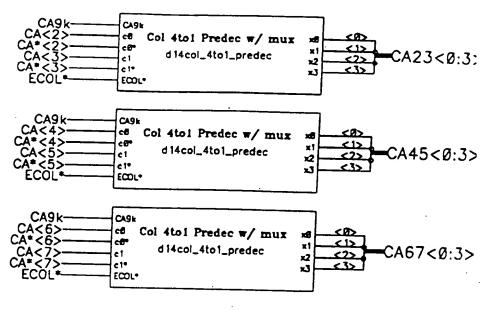


FIGURE 129

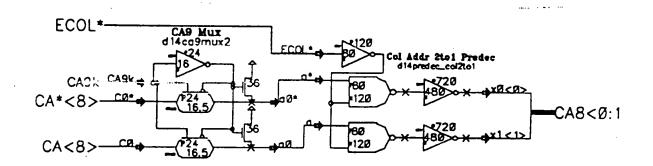


FIGURE 130

INPUTS

LSO*<8:1> EO ENPH*<0:1> ENSA* EPSA* RPRE RBPRE REDTESTC PRG916<1,2> PRGCANR DBML*_T DBMR*_T DBMR*_B DBMR*_B POWERUP*

OUTPUTS

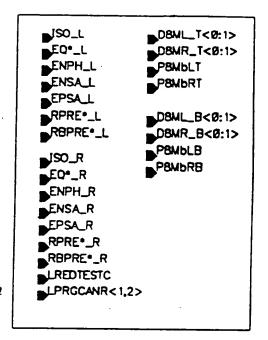
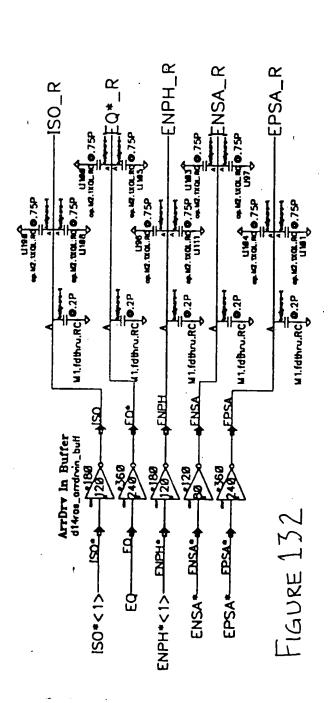
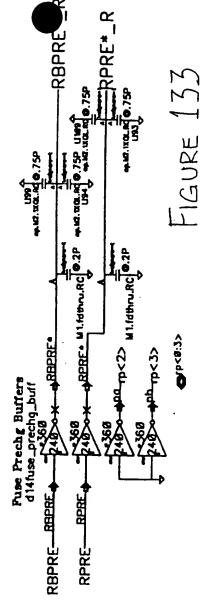


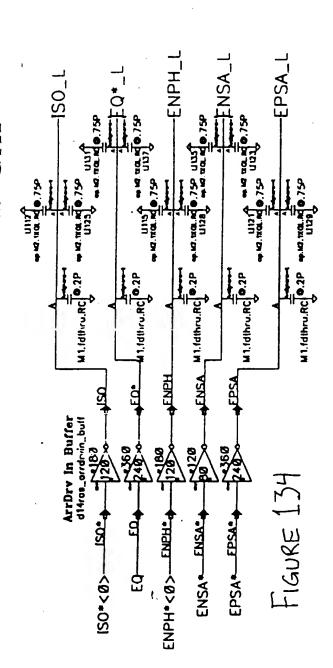
FIGURE 131

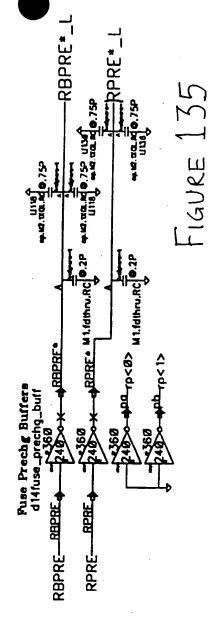
RIGHTSIDE OF PERIPH GAP





LEFTSIDE OF PERIPH GAP





Spare Gates for Topo d14spare_topo

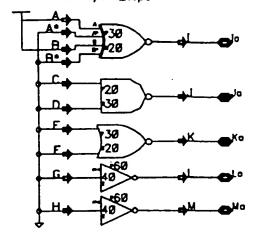


FIGURE 136

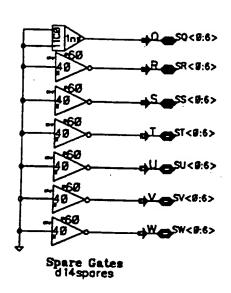


FIGURE 137

Spare Cates for Topo d14spore_topo

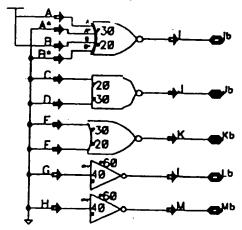


FIGURE 138

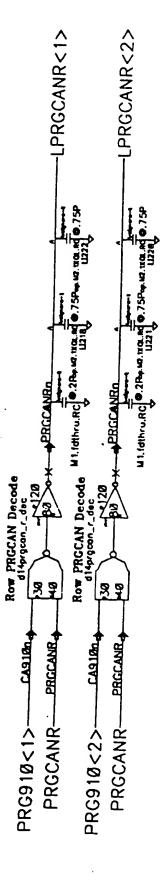


FIGURE 139

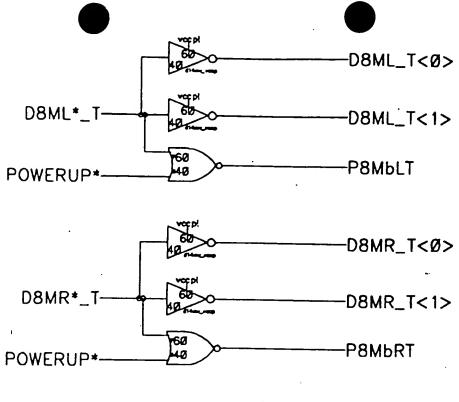


FIGURE 140

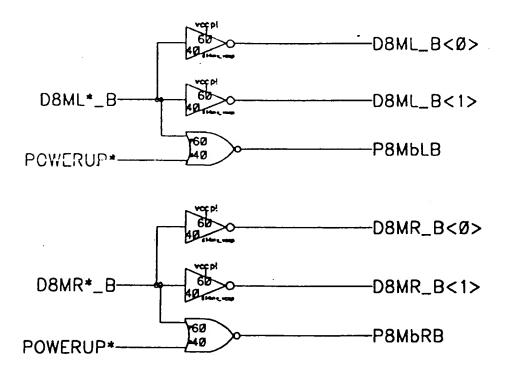
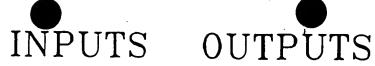
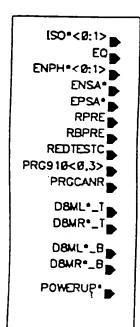


FIGURE 141

REDTESTC Driver
d 14redtestc_drv

REDTESTC REDIESIC LREDTESTC





JSO_L EQ*_L ENPH_L ENSA_L EPSA_L RBPRE*_L JSO_R E0*_R ENPH_R ENSA_R EPSA_R RPRE*_R RBPRE*_R LREDIESIC LPRGCANR<0,3:	DBML_T<Ø:1> DBMR_T<Ø:1> PBMbLT PBMbRT DBML_B<Ø:1> DBMR_B<Ø:1> PBMbLB PBMbRB

LEFTSIDE OF PERIPH GAP

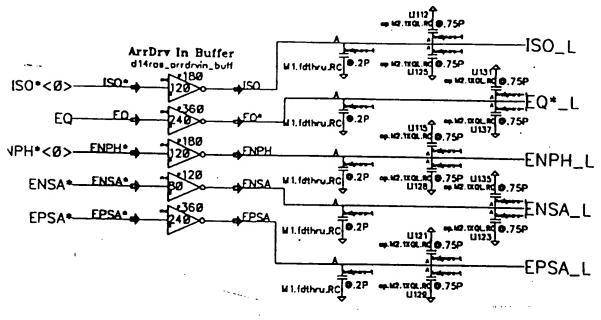


FIGURE 144

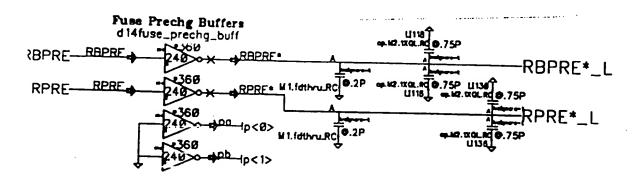


FIGURE 145

RIGHTSIDE OF PERIPH GAP

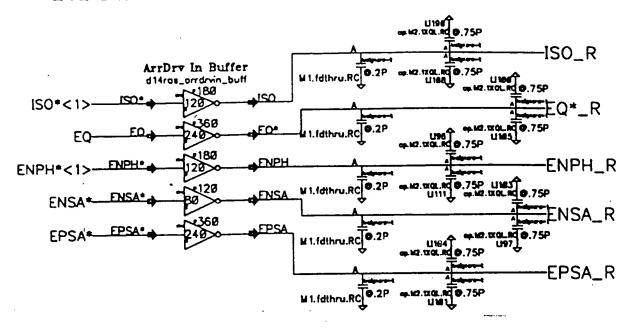


FIGURE 146

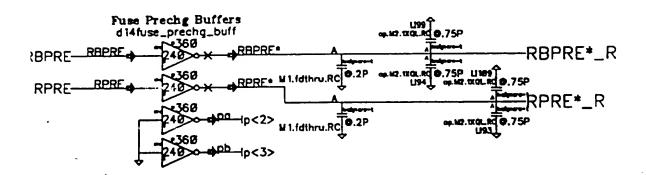
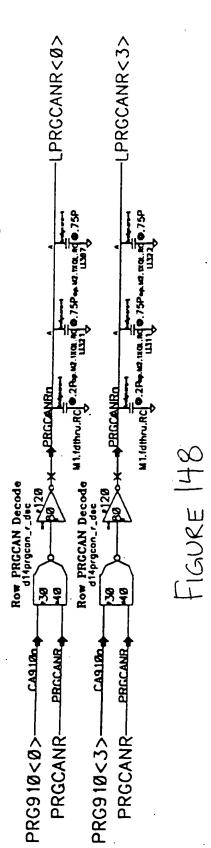


FIGURE 147



VCCP DIODE CLAMPS

414vcp_dia_clomp

414vcp_dia_

FIGURE 149

REDIESTC Driver
discretente.dry

REDIESTC BEDIESTC + 128 ALBEDIESTC LREDIESTC

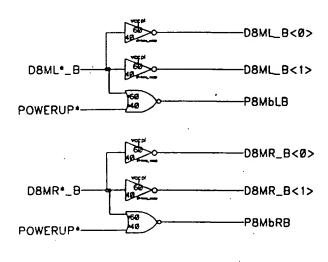


FIGURE 151

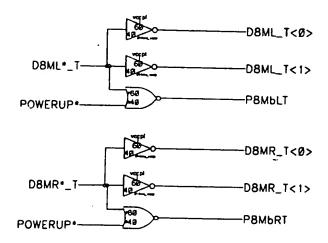


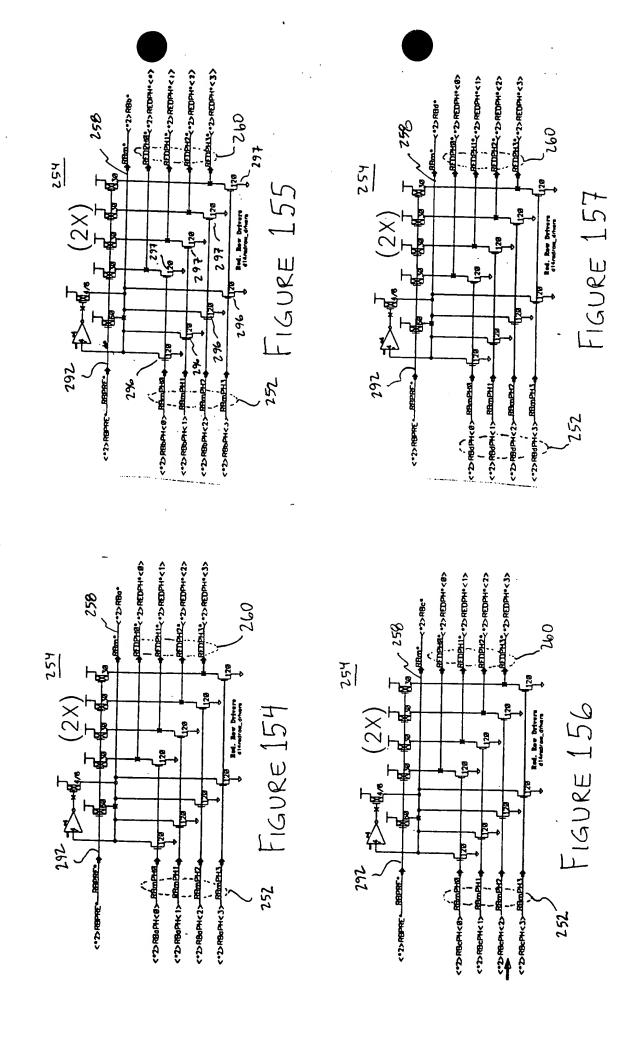
FIGURE 152

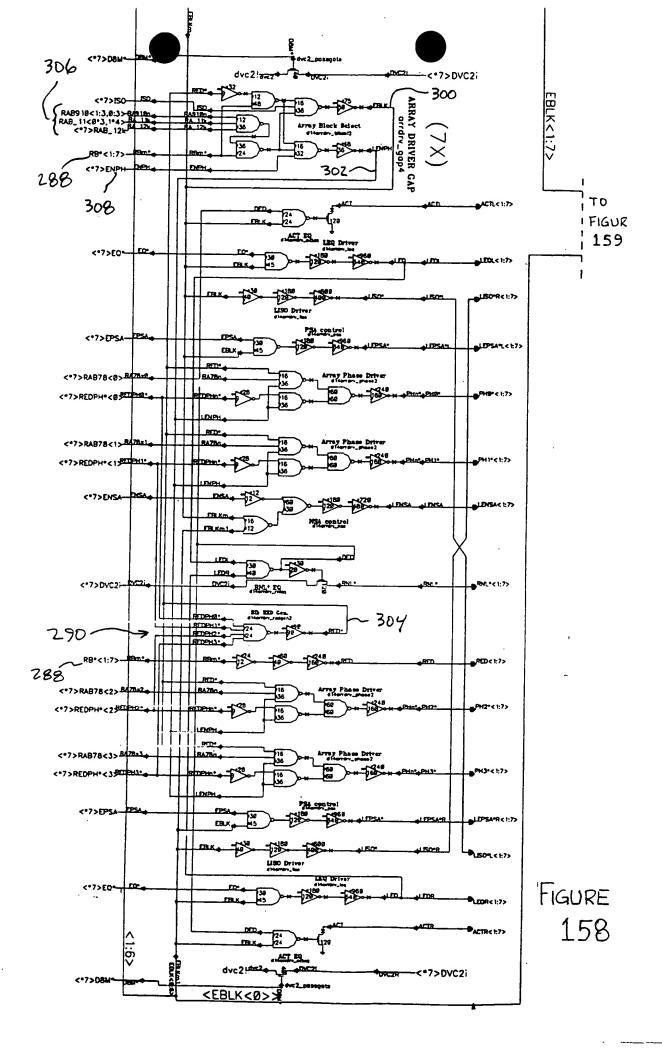
INPUTS

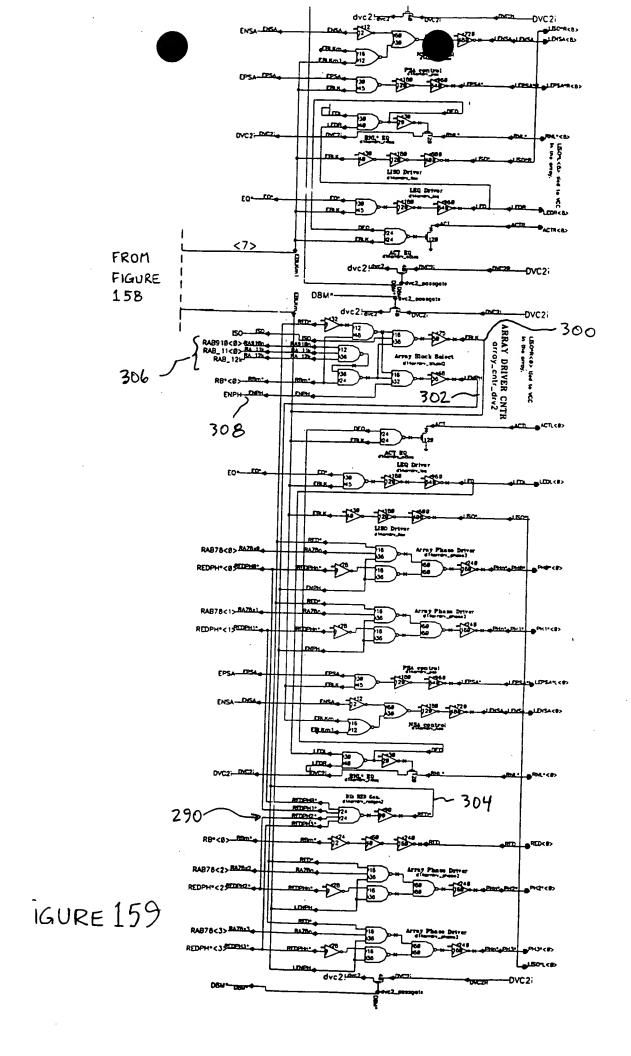
RBoPH<0:3>	150
RBbPH<0:3>	EO•
RBcPH<0:3>	ENPH
RBdPH<0:3>	ENSA
RB*<0:7>	EPSA RBPRE•
DBM*	RAB78<0:3>
	RAB910<0:3>
	RAB_11<0:1>
	RAB_12k

RBg*
RBg*
RBg*
RBg*
RBg*
RBd*
REDPH*<0:3>

FIGURE 153







Gap PSA Driver 500 FIGURE 160

Gap PSA Driver

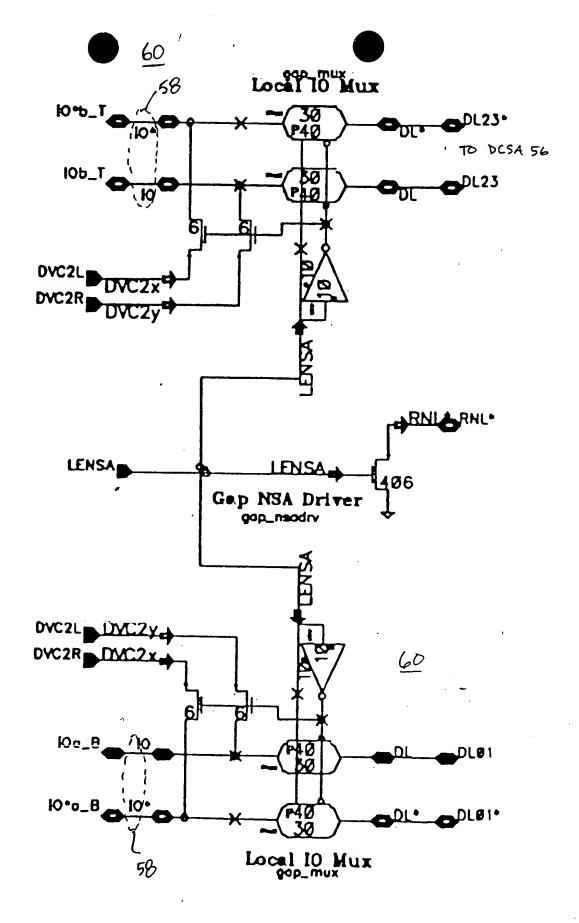


FIGURE 162

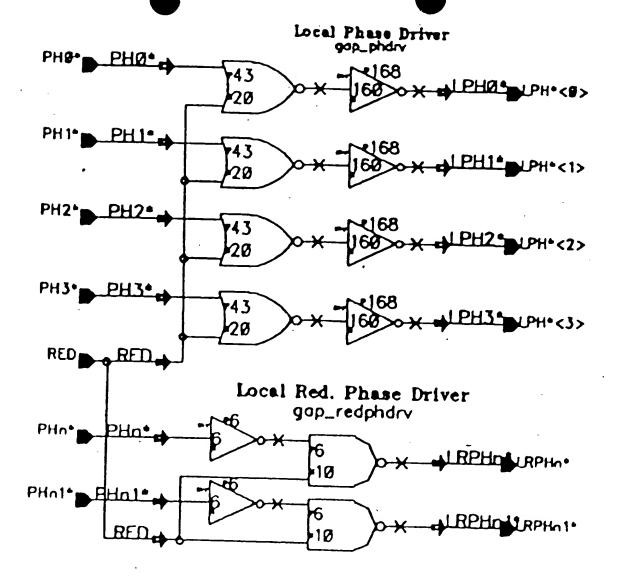


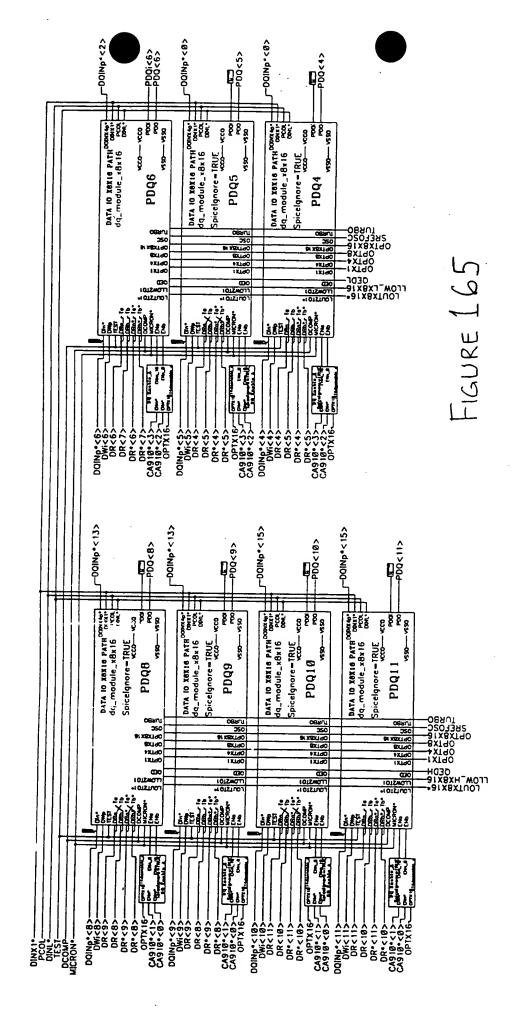
FIGURE 163

INPUTS

DQINp°<0.2,13,15> DINX1° DINX1° PCOL DINL° PCOL OEDH EQSA° OFDL SREFOSC OPTS DR<4:11>OPTEDO DR°<4:11>OPTEDO DR°<4:11>OPTX1 CA910<0:3>OPTX4 TRISTATE° DOUTL° OPTX16 DCOMP MICRON° TEST

OUTPUTS

DW<4:11>
PDQ<4:11>
CA910*<0:3>



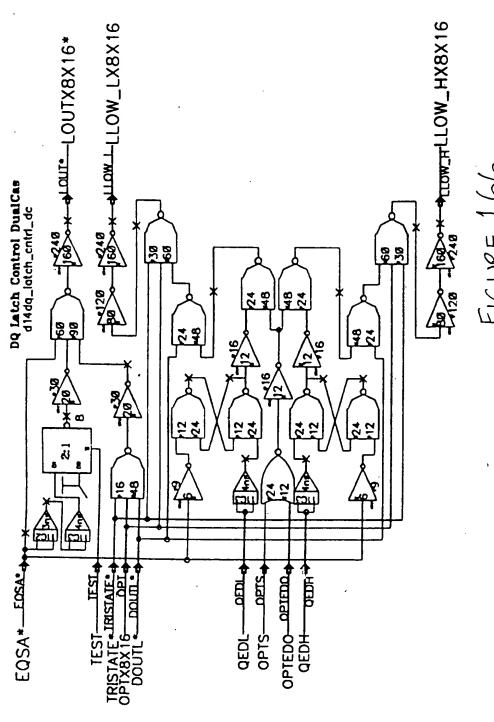
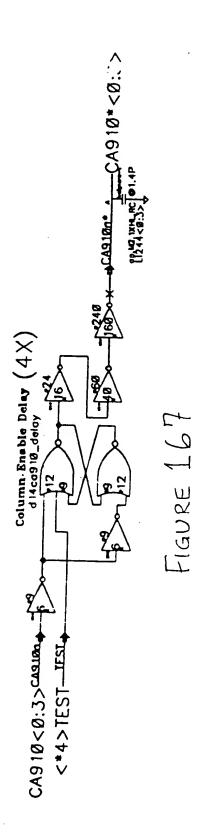


FIGURE 166



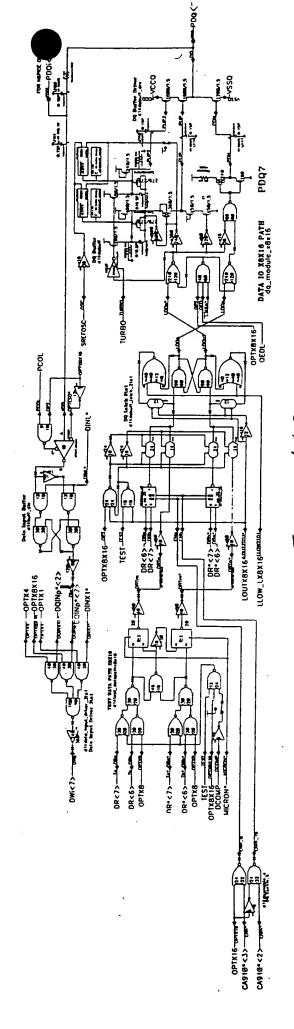
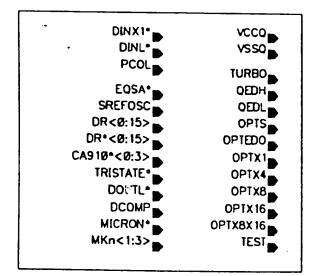


FIGURE 168

X8/X16 DQ Pads (DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11)

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	DŴ	DR/DR*
ĎQ1	DQØ	Ø	Ø 1	Ø, 1 Ø, 1
DQ2	DQ1	2 3	2 3	2, 3 2, 3
DQ3	DQ2	4 5	4 5	4, 5 4, 5
DQ4	DQ3	6 7	6 7	6, 7 6, 7
DQ5	DQ4	8 · 9	8 9	8, 9 8, 9
DQ6	DQ5	1Ø 11	1Ø 11	1Ø, 11 1Ø, 11
DQ7	DQ6	12 13	12 13	12, 13 12, 13
DQ8	DQ7	14 15	14 15	14, 15 14, 15

INPUTS



OUTPUTS

DRn<1:3>
DRn*<1:3>
DRn*<1:3>
TDRn<0:3>
TDRn*<0:3>
DRTn<0>
DRTn<0>
DRTn*<0>
DOINP*<2,13,15>
DW<2,3,12:15>
PDQ<2,3,12:15>

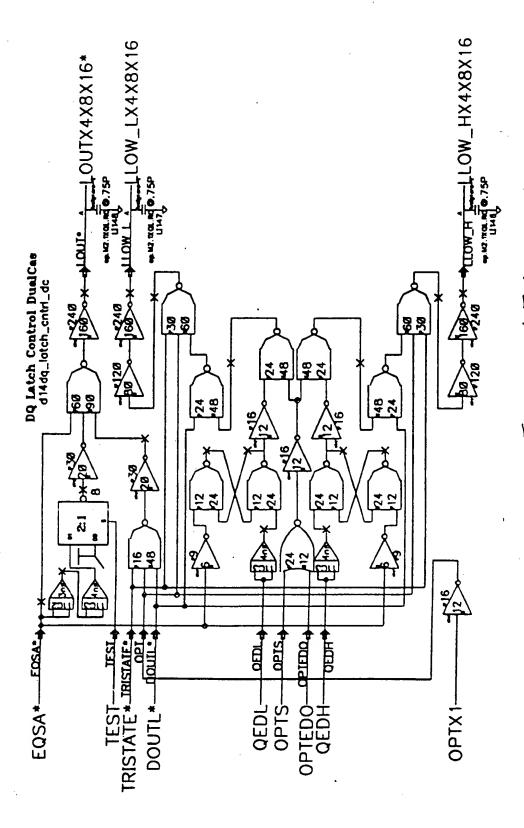


FIGURE 171

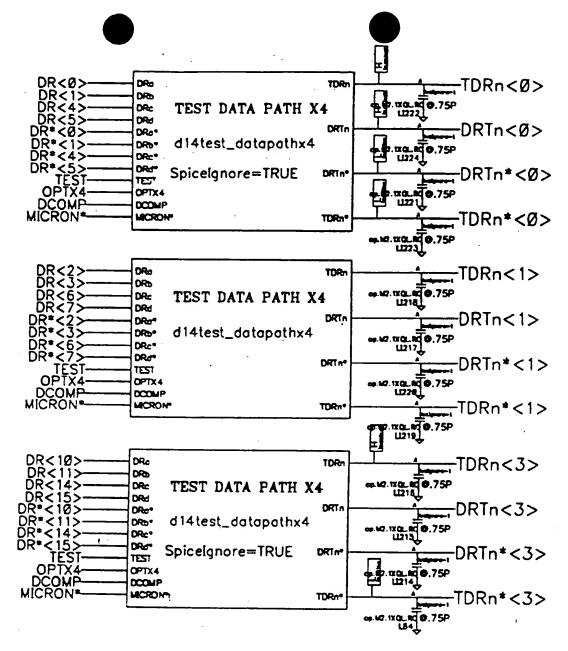
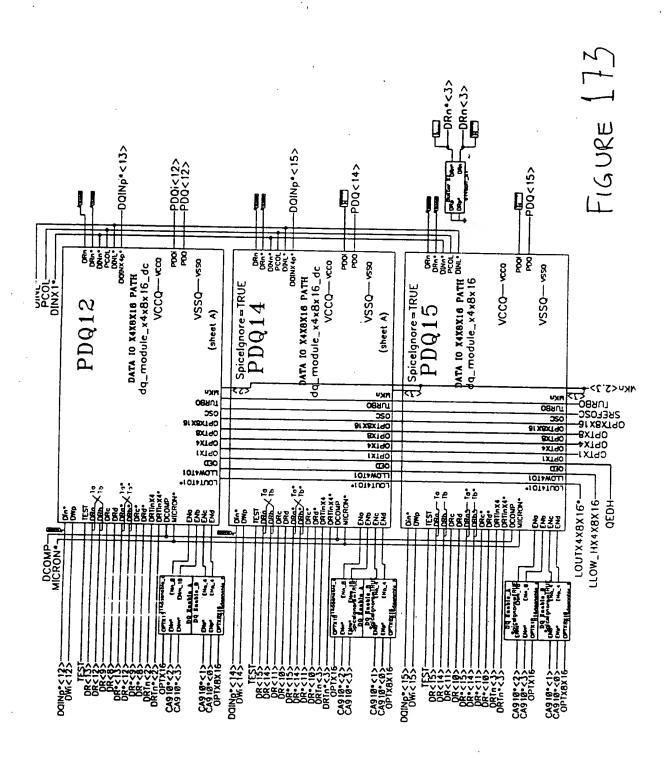
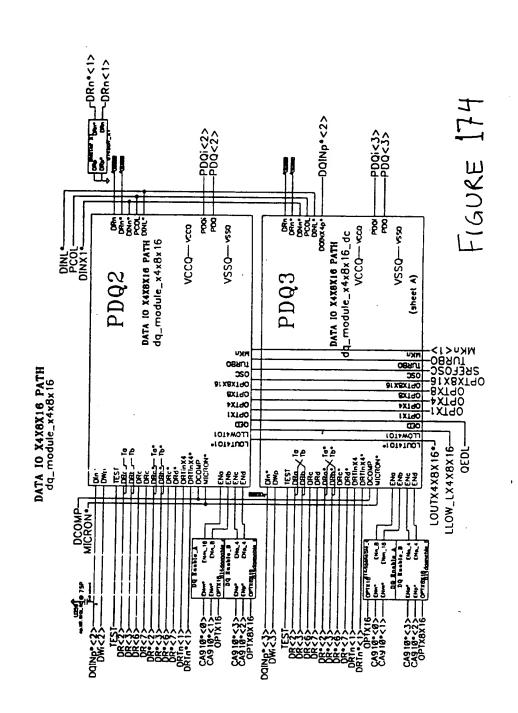
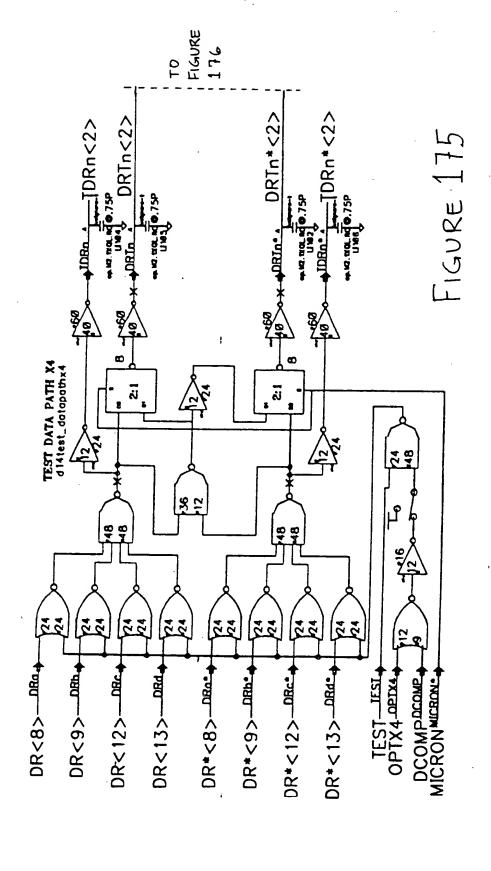


FIGURE 172







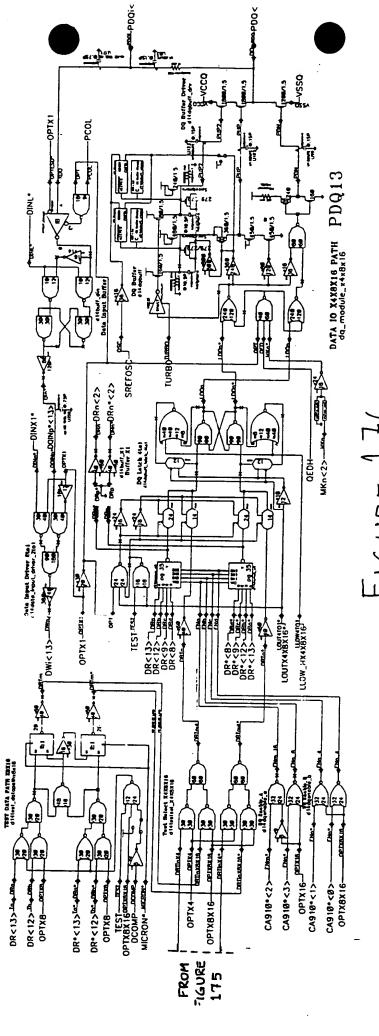
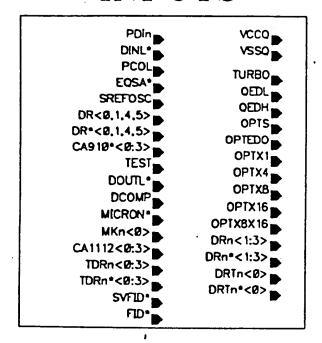


FIGURE 176

INPUTS



OUTPUTS

TRISTATE*
DINX1*
DOINp*<0>
DW<0.1>
PDQ<0.1>

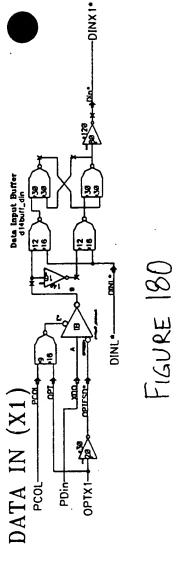
Data Read DR/DR* 0, 1, 4, 5 2, 3, 6, 7 2, 3, 6, 7 2, 3, 6, 7 8, 9, 12, 13 8, 9, 12, 13 10, 11, 14, 15	X4 Configuration	ration				X1 Cor	X1 Configuration (see next page)	next page)	
DQØ Ø Ø Ø I F DRn<8> 1 1 1 0 I 4 5 E DRn<8> 0Q1 2 2 6 7 2 3 6 7 E DRn<1> DRn<1> DRn<1> DRn<2	Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	Data Write DW	Data Read DR/DR*	:	3/0R•	Bond Pad	Assembly Pin-out
DQ1 2 2, 6, 7 2, 3, 6, 7	100	800	0	0, 4, 5	0, 1, 4, 5	4	Rn<0>		5
DQ1 2 2, 6, 7 2, 3, 6, 7 Ponctor DQ2 12 12 13, 8, 9 8, 9, 12, 13 DQ3 14 14 14 16, 11, 14, 15			-	-	0.1.4.5			- PDOB	
DO2 12 12 8, 9, 12, 13	000	5	. 2	2, 6, 7	2, 3, 6, 7	4	Ru<1>	<u></u>	
DQ2 12 12 8, 9, 12, 13 B DRn<2> DQ3 14 14 16 16, 11, 14, 15 B DRn<3> DQ3 15, 10, 11 10, 11, 14, 15	046	3	3	3	2. 3. 6. 7		 		
DQ3 15, 16, 11 16, 15 B DRA<2>	100	200	12	12	8, 9, 12, 13				
DO3 14 14 15 18, 11, 14, 15 15 15 15 15 15 15 15 15 15 15 15 15	0.63	700	13	13, 8, 9	8. 9. 12. 13		Ruc 2 >		
15 15, 10, 11 10, 11, 14, 15	P O0	200	41	14	10, 11, 14, 15	· 			,
	100	663	15	15, 10, 11	10. 11. 14. 15	4	20 13 -		

FIGURE 178

DQ Compression

DR/DW	PDQ	V8 DQ	X16 D0
0,1,4,5	1,0	6	0
2,3,6,7	2,3	-	2
8,9,12,13	12,13	9	13
10,11,14,15	14,15	7	15

FIGURE 179



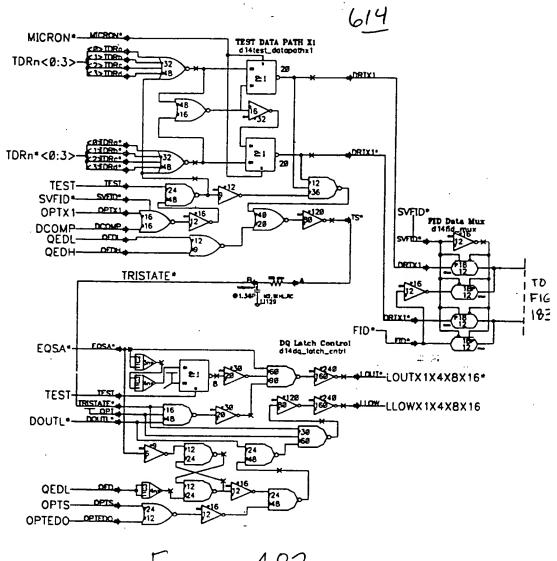


FIGURE 182

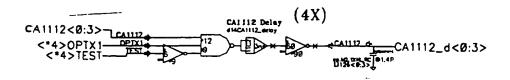
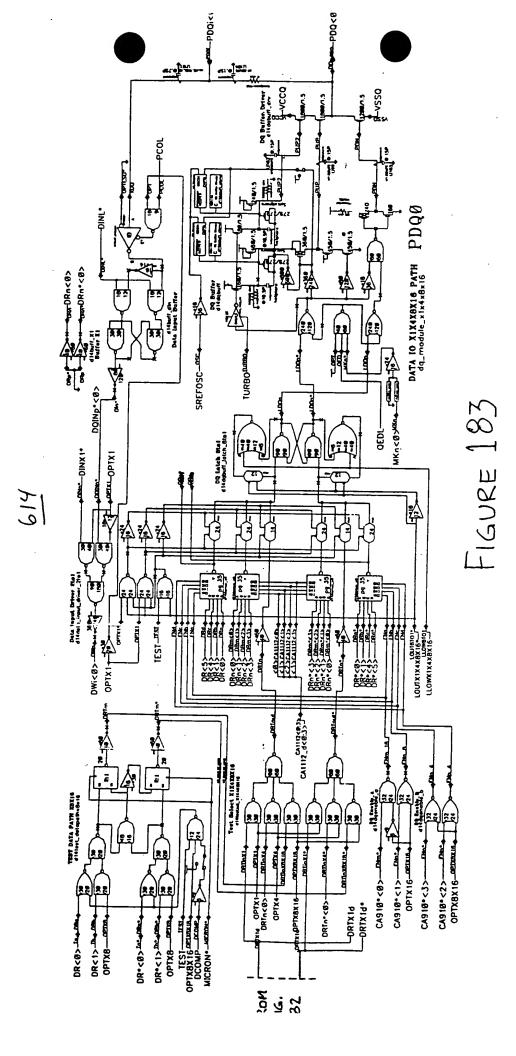
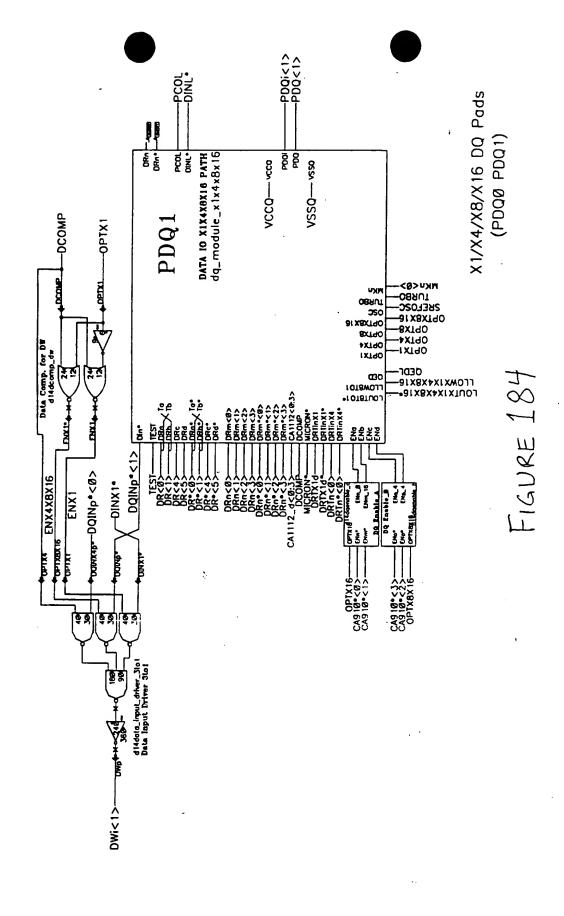
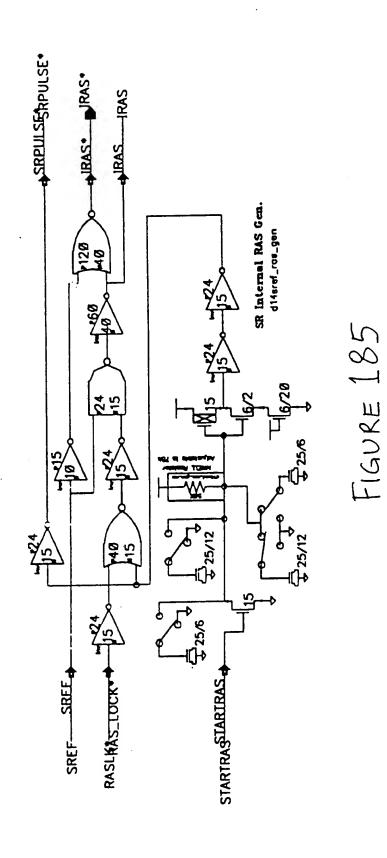


FIGURE 181







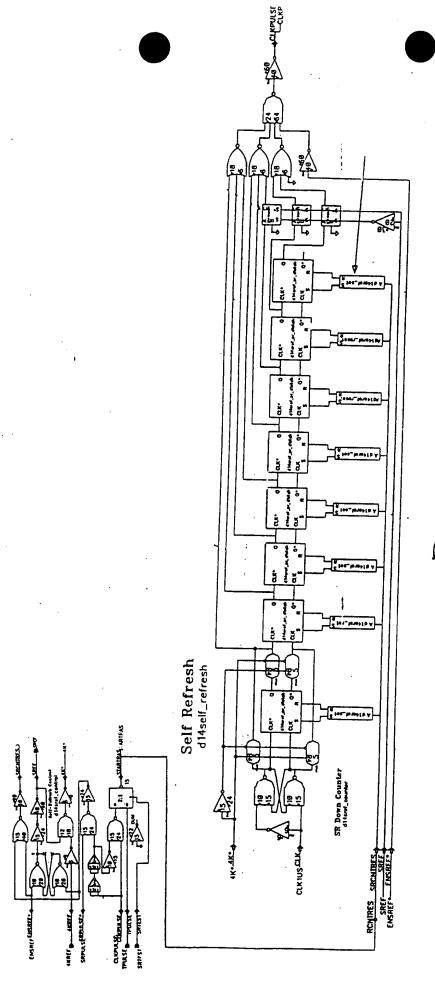
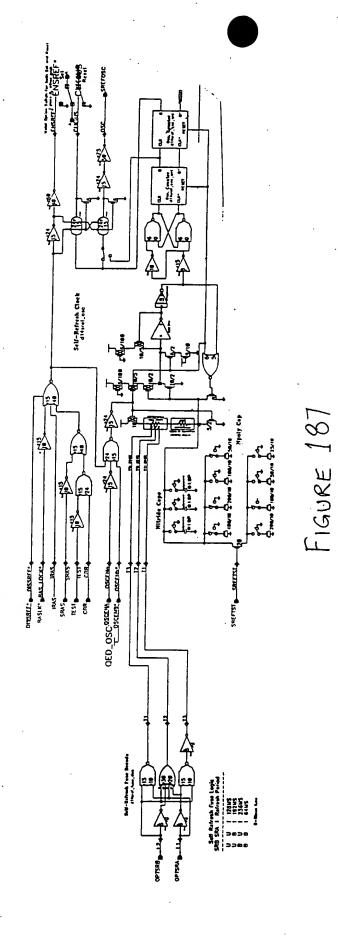
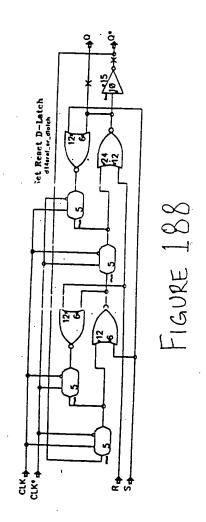
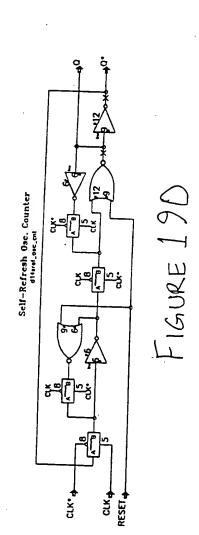


FIGURE 186





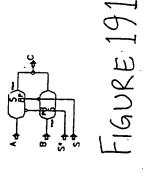


Metal Option Sales for both Saf and Parret

R SSet

Reset

FIGURE 1899



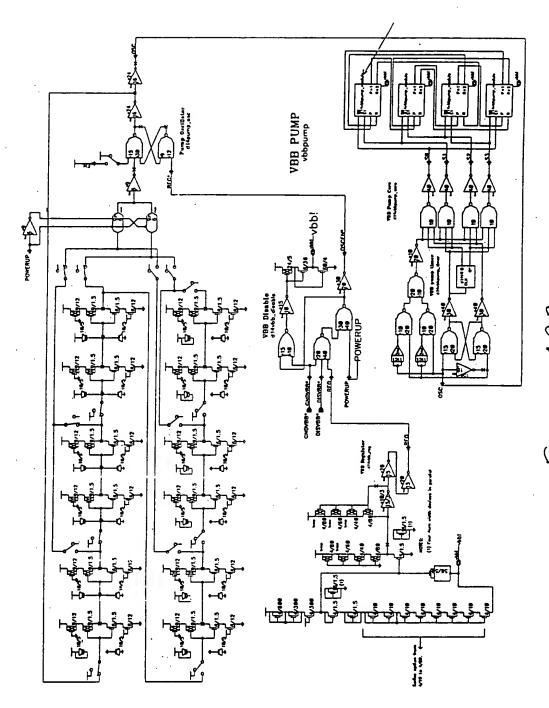
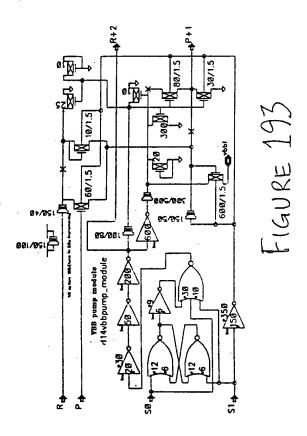
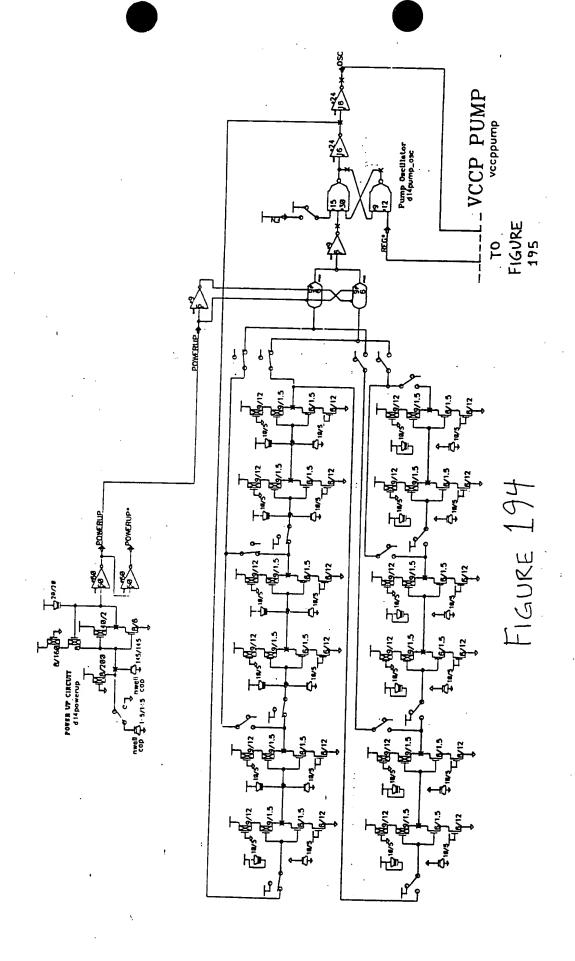
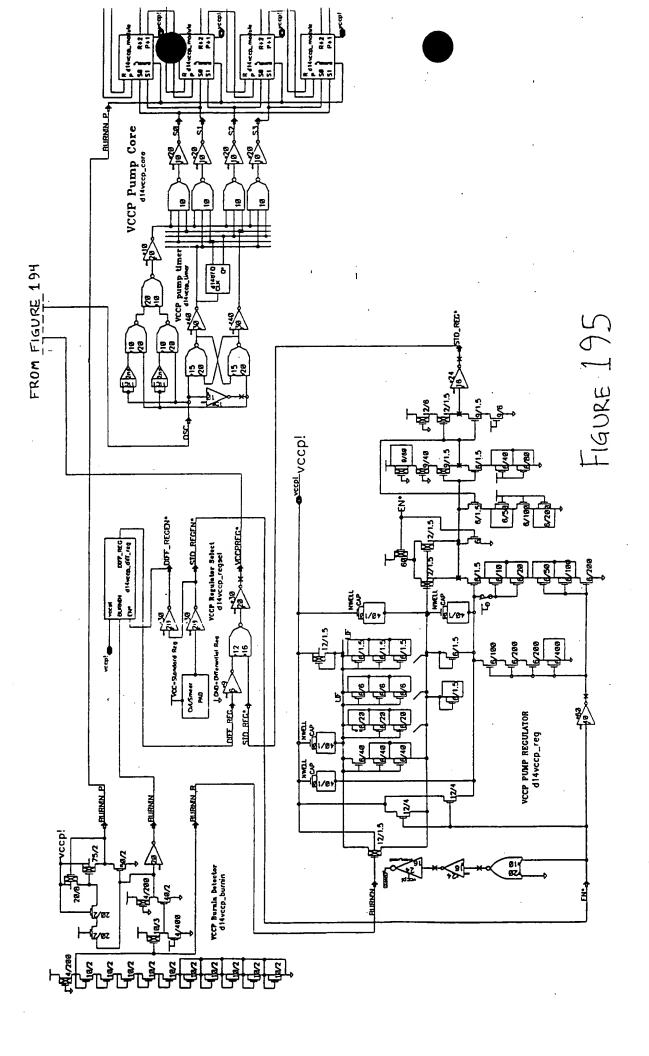


FIGURE 192







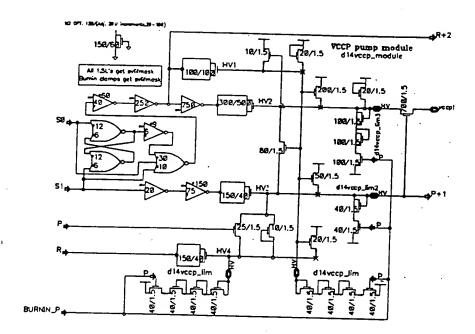
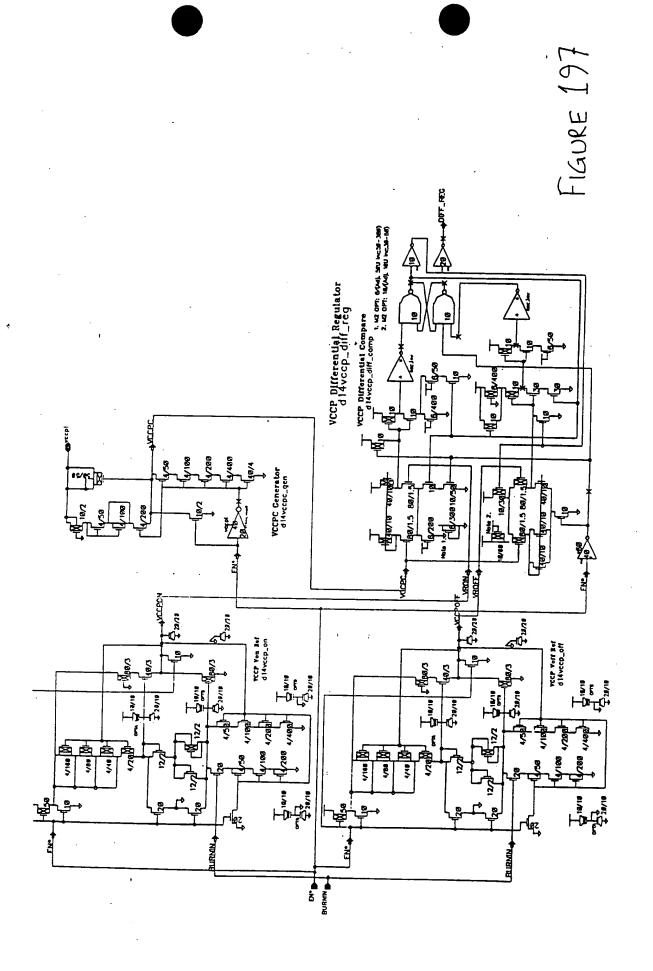


FIGURE 196



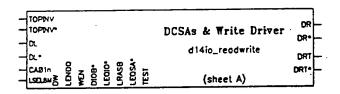
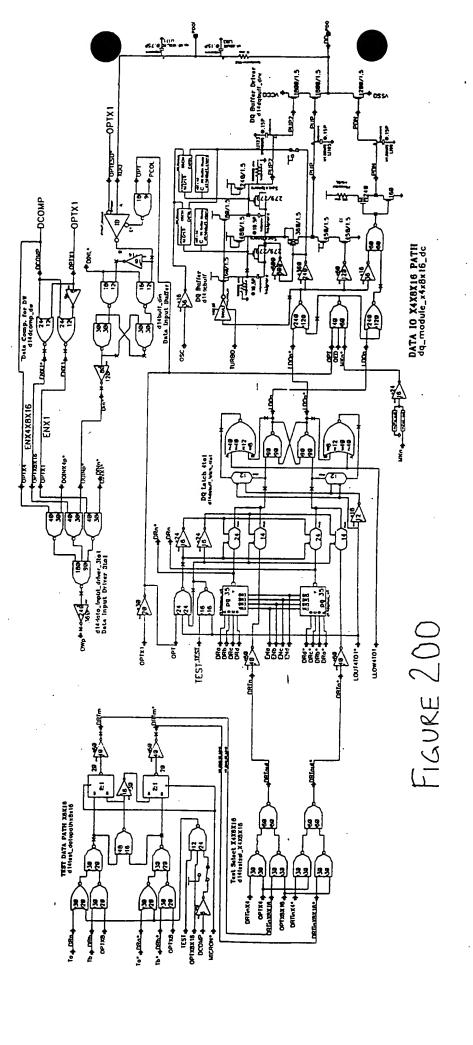
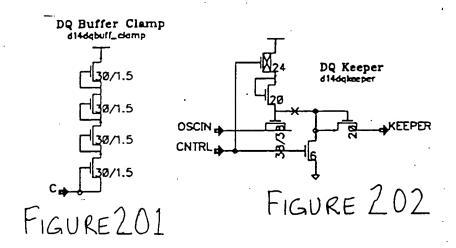


FIGURE 198

```
| Din* |
```

FIGURE 199





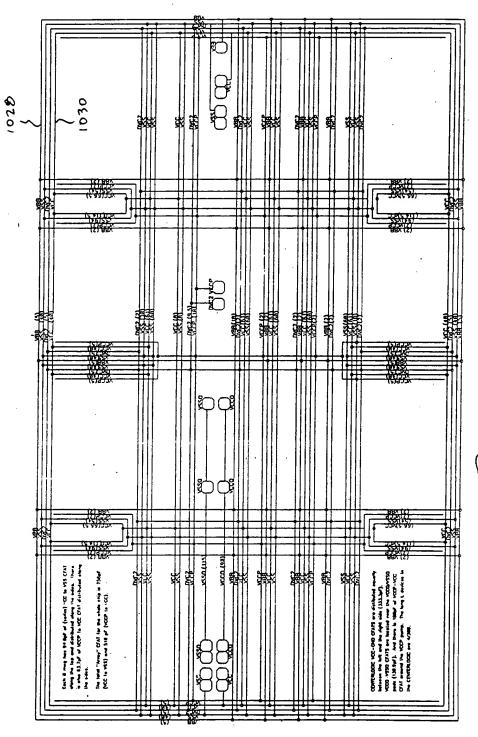


FIGURE 203

CONFIG	ROW A	DDRESS	COLUMN	ADDRESS
	8K refresh	4K refresh	8K refresh	4K refresh
	AØ - A12	· · · ·	AØ - A8	AØ - A9
8MX8	AØ - A12	AØ - A11	AØ - A9	AØ - A1Ø
16MX4	AØ - A12	_	AØ - A1Ø	AØ - A11
64MX1	AØ - A12	_	AØ - A12	<u> </u>

FIGURE 204

Test M	ode Address Compression (ref to X1)				
The following column addresses are ignored					
. 16X	A12, A11, A10, A9				
32X	A12, A11, A10, A9, A8 (defoult customer testmode)				
64X	A12, A11, A10, A9, A8, A7				
128X	A12, A11, A10, A9, A8, A7, plus row address A12				

DQ Configuration

	(X16)	(X8)	(X4)	(X16)	(X8)	(X4)	(X1)
	DQ5	DQ2 (DQØ	DQ4	DQ2	DQØ])CA1112<Ø>
	DQ7	DQ3	DQ1	DQ6	DQ3	DQ1])CA1112<1>
	DQ13	DQ6	DQ2	DQ12	DQ6	DQ2])CA1112<2>
	DQ15	DQ7	DQ3	DQ14	DQ7	DQ3])CA1112<3>
	<u>-</u>			·			<u> </u>
	•	CA910<2	>	(CA910<3	>	
ļ	DQ1Ø	DQ5	DQ3	DQ11	DQ5	DQ3	
							CA1112<3>
	DQ1Ø	DQ5	DQ3	DQ11	DQ5	DQ3	┤ {
	DQ1Ø	DQ5	DQ3	DQ11	DQ5	DQ3	CA1112<2>

FIGURE 206

X8 Configuation

			_	
Assembly Pin-out	Schematic Pin-out	Bond Pud . PDQ	DW	DR/DR*
DQ1	DQØ	Ø 1.	Ø 1	Ø, 1 Ø, 1
DQ2	DQ1	2 3	2 3	2, 3 2, 3
DQ3	DQ2	4 5	4 5	4, 5 4, 5
DQ4	DQ3	6 7	6 7	6, 7 6, 7
DQ5	DQ4	89	8 9	8, 9 8, 9
DQ6	DQ5	1Ø 11	1Ø 11	1Ø, 11 1Ø, 11
DQ7	DQ6	12 13	12 13	12, 13 12, 13
DOB	DQ7	14 15	14 15	14, 15 14, 15

(DOOT) Bond Pad Assembly PDQ Pin-out PDO0 X1 Configuration ◆ DRn<0> ◆ DRn<1> ◆ DRn<2> → DRn<3> DR/DR. 10, 11, 14, 15 10, 11, 14, 15 8, 9, 12, 13 8, 9, 12, 13 Data Read DR/DR• 9, 1, 4, 5 0, 1, 4, 5 2, 3, 6, 7 Data Write DW 15, 10, 11 13, 8, 9 0, 4, 5 2, 6, 7 2 Bond Pod PDQ 4 5 2 0 Schematic Pin-out X4 Configuration DOØ 001 **DQ2** 003 Assembly Pin-out 004. 00 003 002

FIGURE 208

DQ Compression

	X8	X8 Config	X16	X16 Config
DR/DW	PDQ	Assembly DQ	PDQ	Assembly DQ
0,1,4,5	1'0	-	Ø	-
2,3,6,7	2,3	2	2	ю
8,9,12,13	12,13	7	13	4
10,11,14,15	14,15	80	15	16

FIGURE 209

Address Compression

CONFIG	ROW ADDRESS	COLUMN ADDRESS	Г
	8K ref 4K ref	8K ref 4K ref	
4MX16	AB - A12 AB - A11		0
8MX8	A0	A A A A	5
16MX4	AB - A12 AB - A11	1 10 V	
64MX1	- A12	- A12	=

FIGURE 210

				,
Test Mode Address Compression (ref to X1) The following column addresses are ignored	A12, A11, A10, A9	A12, A11, A10, A9, A8	A12, A11, A10, A9, A8, A7	A12, A11, A10, A9, A8, A7, RA12
Test Mod The follov	16X	32X	64X	128X

Cancel Row Fusebank

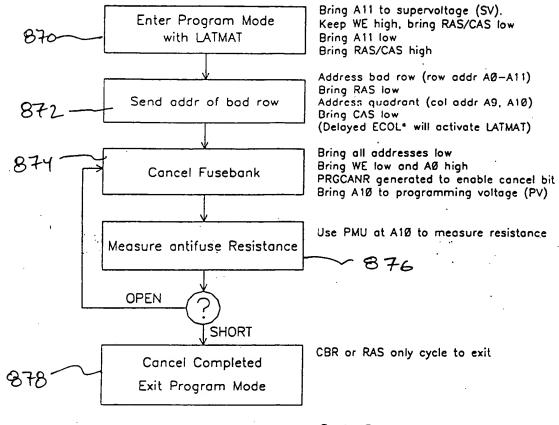
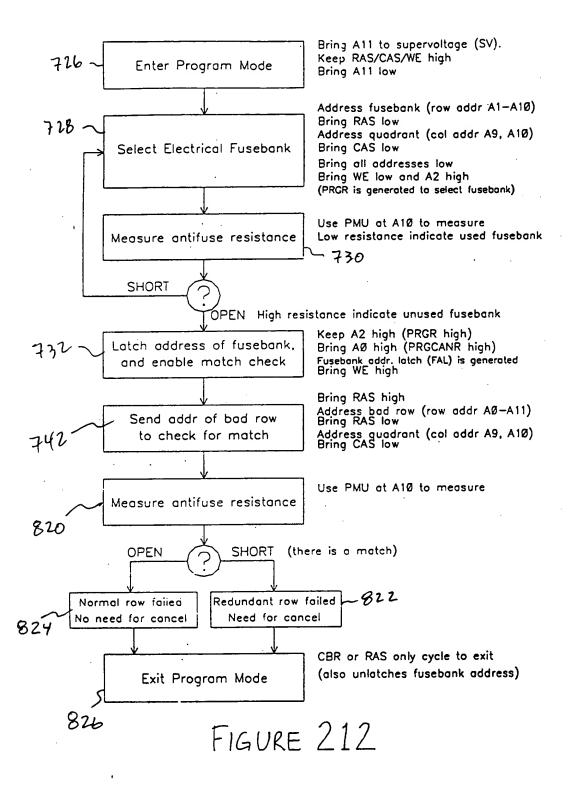
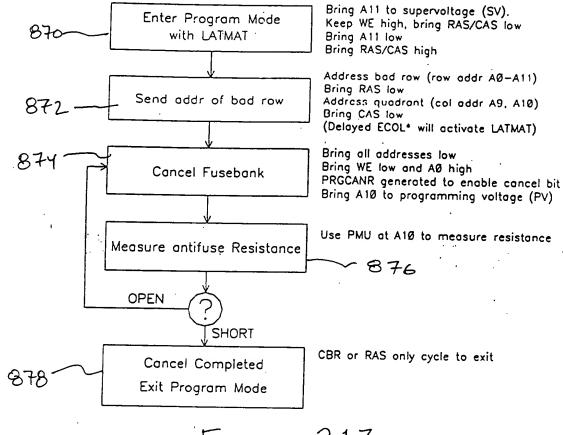


FIGURE 213

Locate Usable Electrical Fusebank and Determine Need for Cancel



Cancel Row Fusebank



Program Row Fusebank

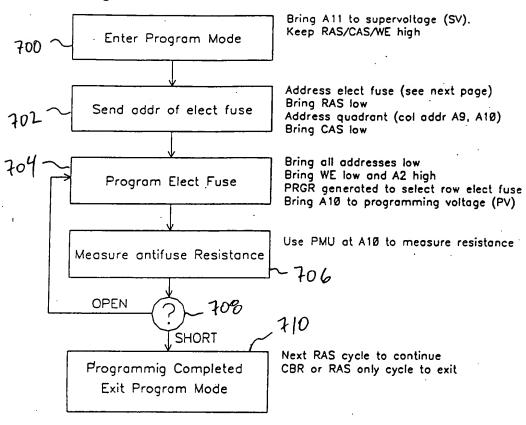


FIGURE 214

Determine Need for Cancel

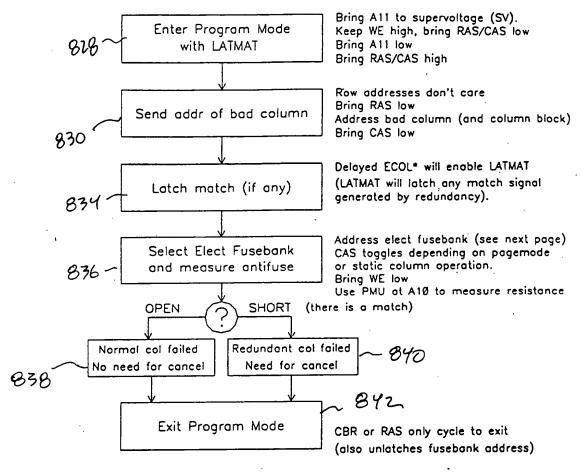


FIGURE 215

Program Column Fusebank

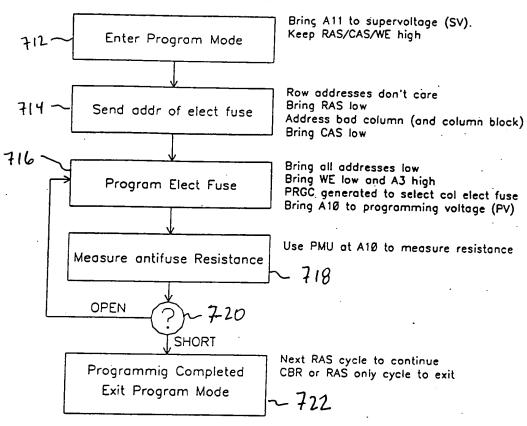


FIGURE 216

Cancel Column Fusebank

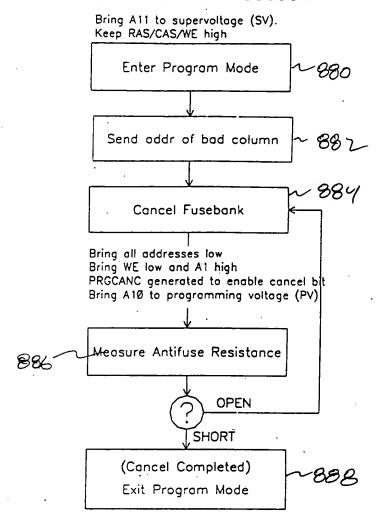
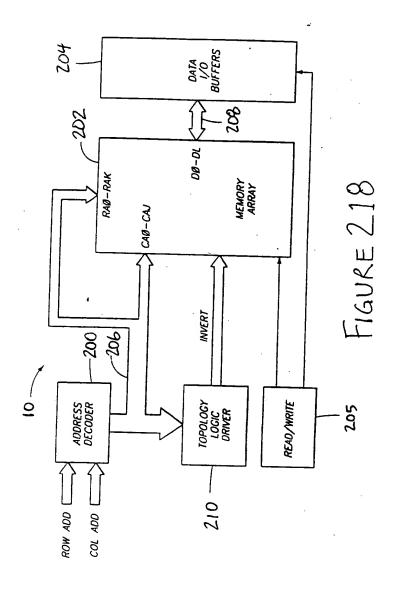
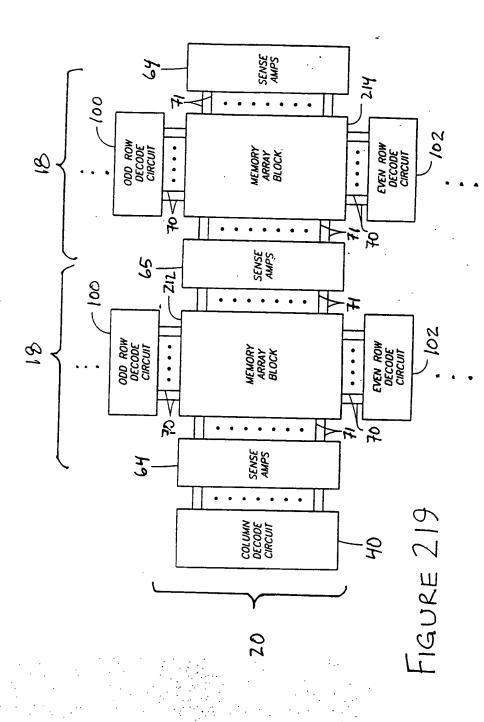


FIGURE 217





		, _		8771	0 00	010	02 0	030	02 1	03 1	1 00	1 10			
	RA8=1	RA8=1	0	_	R770	01 1	1 00	03 1	1 20	030	020	0 10	0 00		
			_	0	R769	1 10	1 00	03 1	1 20	030	0 70	0 10	0 00		
TWIST		0	0	R768	0 00	0 10	0 70	03 0	02 1	03.1	1 00	1 10			
	RA8=Ø	,		R515	1 10	0 00	03 1	020	030	02 1	0 10	1 00			
		0	`	R514	1 00	0 10	02 1	030	0 20	03.1	0 00	1 10	_		
		ZZ.	RA	_	0	R513	1 00	0 10	02 1	030	0 20	03 1	0 00	1 10	
		0	0	R512	1 10	0 00	03 1	0 70	030	02 1	0 10	1 00	-		
		RAØ	RAI	·		C42=0				CA2=1			_		

FIGURE 22D

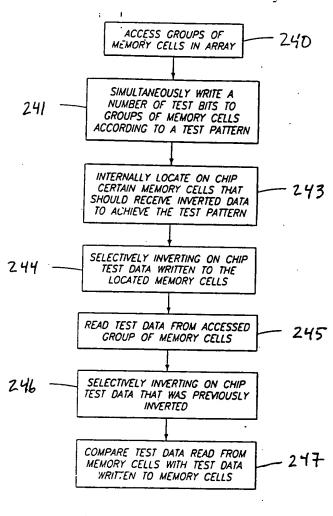
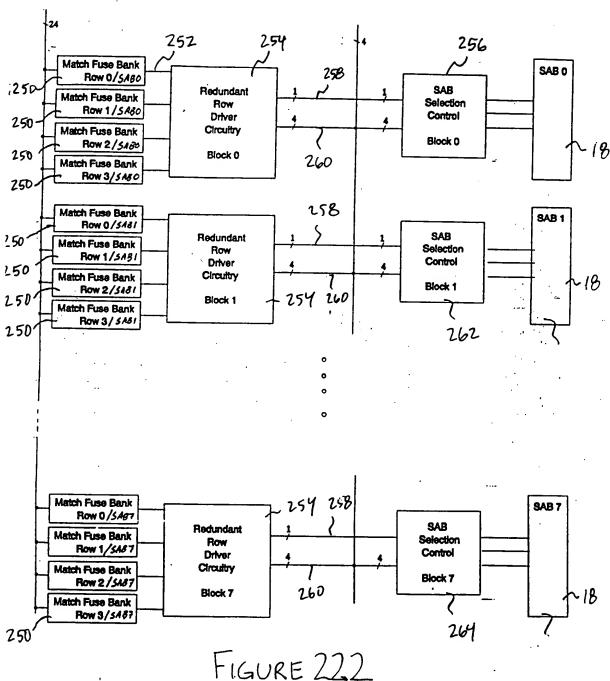
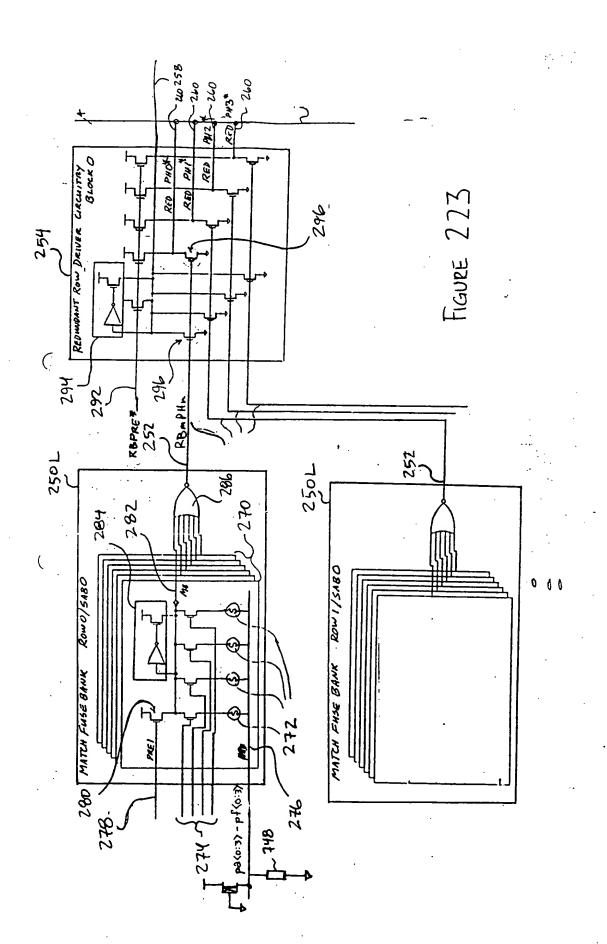
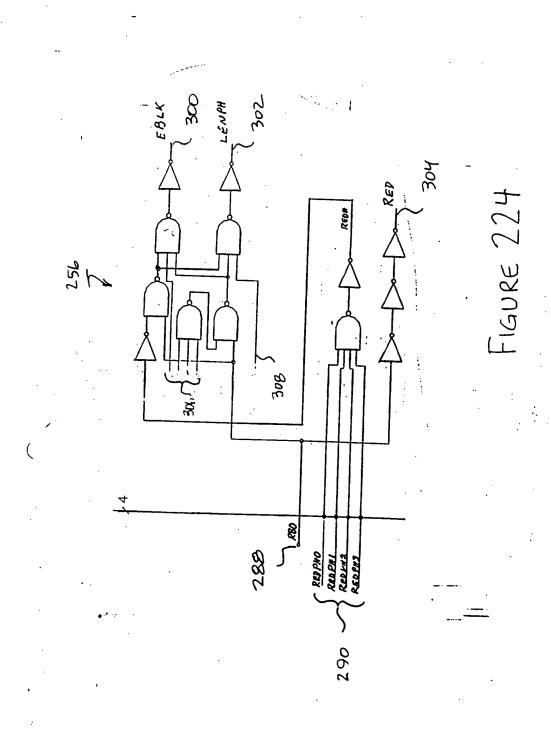


FIGURE 221

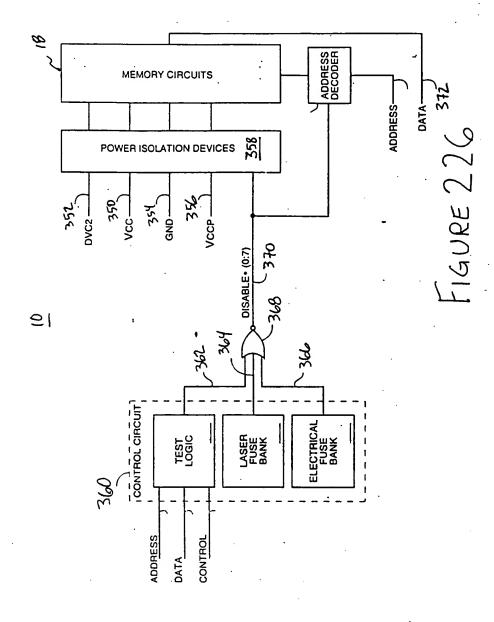




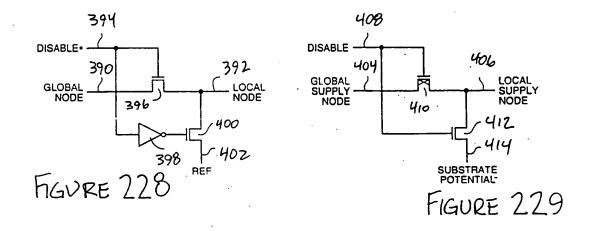


	SAB0											
OP	ERATION	TYPE		SELECTION CONTROL								
				Input			Output					
Primary Row to Fire ?	Redundant Row In SAB0 7	Primary Address in SAB0 ?	Primary Address Lines	One of REDPHO- REDPH3	RBO	EBLK	LENPH	RED				
	X 10 10 10 10 10 10 10 10 10 10 10 10 10	yes	1	1	1	1	1	0				
yes		no	0	1	1	0	0	0				
		увэ	1	0	0	1	1	1				
l	уез	ino	0	0	0	1	1	1				
no		yes	1	0	1	0	0	0				
	no	no	0	0 or 1*	. 1	0	0	; o				

Depending on whether redundant row in another SAB is to fire







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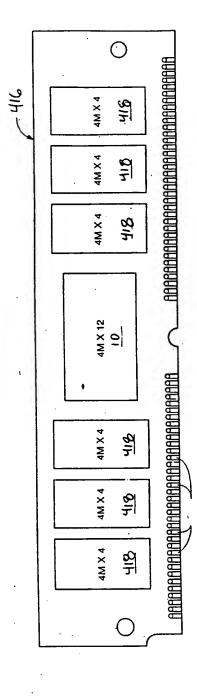
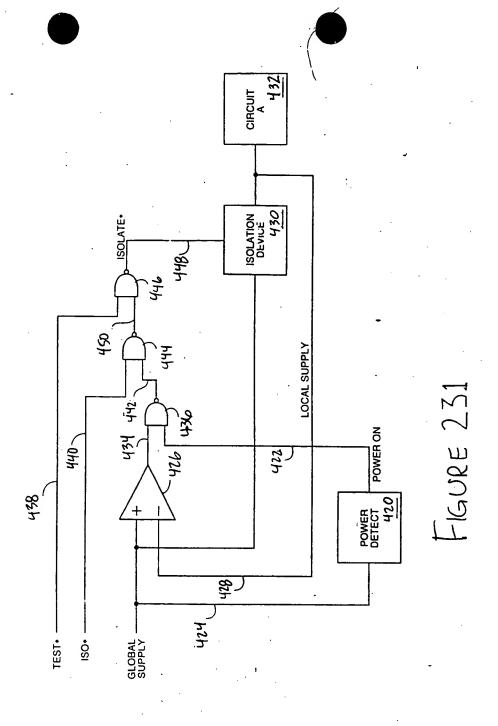


FIGURE 230



Anti-fuse not blown, Address=Ø Anti-fuse blown, Address=1

Row Antifuse Selection Within Each Bank

Fi	ise S	elect	ion	Add	ress	Repair Address=1
	A4	A3	A2	A1		
	Ø Ø	Ø	Ø	Ø 1		A1 A2
	Ø Ø	Ø	1 1	Ø 1		A3 A4
	Ø	1	Ø	Ø 1.		A5 A6
	. Ø	1	1	Ø 1		A7 A8
٠	1 1	Ø	Ø	Ø 1	•	A9 A1Ø
	1 1	Ø	1	Ø 1		AØ A11
	1	1 1	Ø	Ø 1		Enable Bank
	1	1	1	Ø 1		

Row Fusebank Enable Selection

Row F Fusebank	useb A	ank 1ØAS	Sel A8	ecti A7	on A6	Add A5	ress
RØ R1 R2 R3 R4 R5 R6 R7			000000000000000000000000000000000000000	Ø Ø Ø 1 1	Ø Ø 1 1 Ø Ø 1	Ø 1 Ø 1 Ø 1	
R8 R9 R10 R11 R12 R13 R14 R15		•	1 1 1 1 1 1	Ø Ø Ø 1 1	Ø Ø 1 1 Ø Ø 1 1	0 1 0 1 0 1 0 1	
LEFT RIGHT	Ø	Ø 1			_		

FIGURE 233

Column Antifuse Selection Within Each Bank

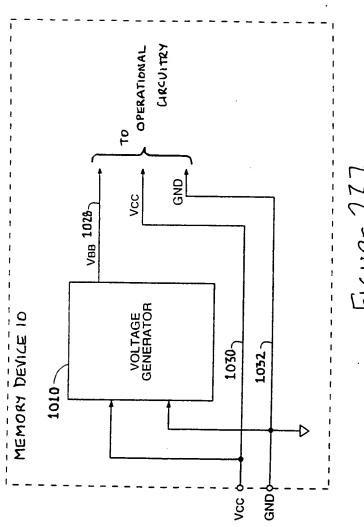
Fuse Se	lectio	n Address	Repair Address=1
A1	AØ	A6	
Ø	Ø	1 Ø	A2 A3
Ø	1 1.	1 Ø	A4 A5
1 1	Ø	1 Ø	A6 A7
1	1	Ø 1	A8 BANK ENABLE

Column Fusebank Enable Selection

Column Fusebank	Fusebank A10.		lection A8	A: A7	
CØ C1	Ø Ø	Ø Ø	Ø	Ø 1	
C2 C3	Ø	Ø Ø	1	Ø 1	
C4 C5	Ø Ø	1 1	Ø Ø	Ø	
C6 C7	Ø Ø	1	1 1	Ø 1	
C8 C9	1	Ø	Ø	Ø	
C1Ø . C11	1 1 1•	Ø Ø Ø	Ø. 1 1	Г Ø 1	
C12	1	1.	Ø	Ø	
C13 C14 C15	1	1 1 1	Ø 1 1	1 Ø 1	e

FIGURE 235

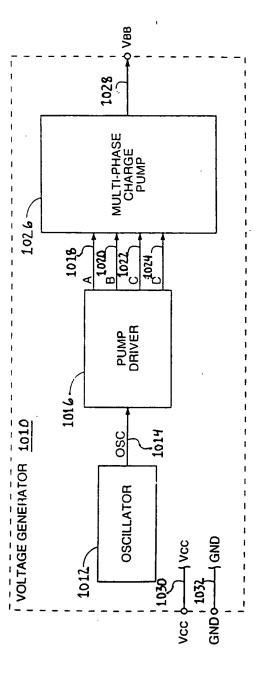
FIGURE 236



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, ,, =

Figure 257



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FIGURE 238

T8 T12 T16 T20 T24 T28 T32

T10 T14 T18 T22 T26 T30

OSC (1014)

A (1018)

B (1020)

C (1022)

D (1024)

P (1094)

FIGURE 239

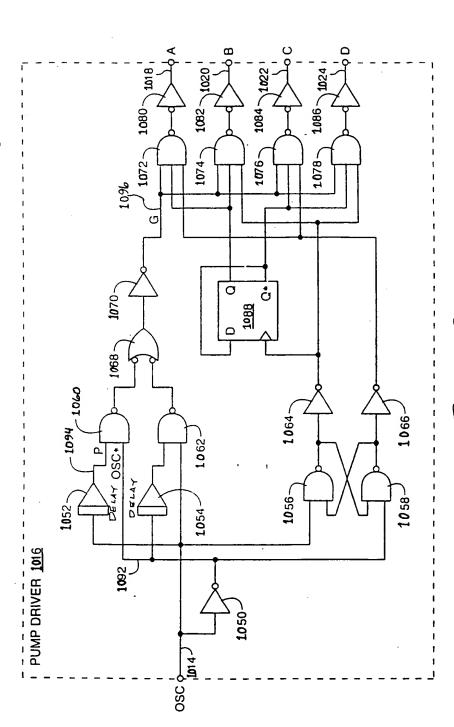
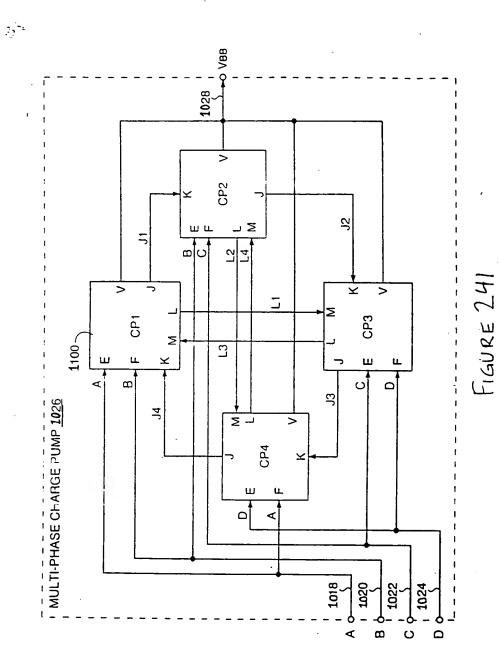
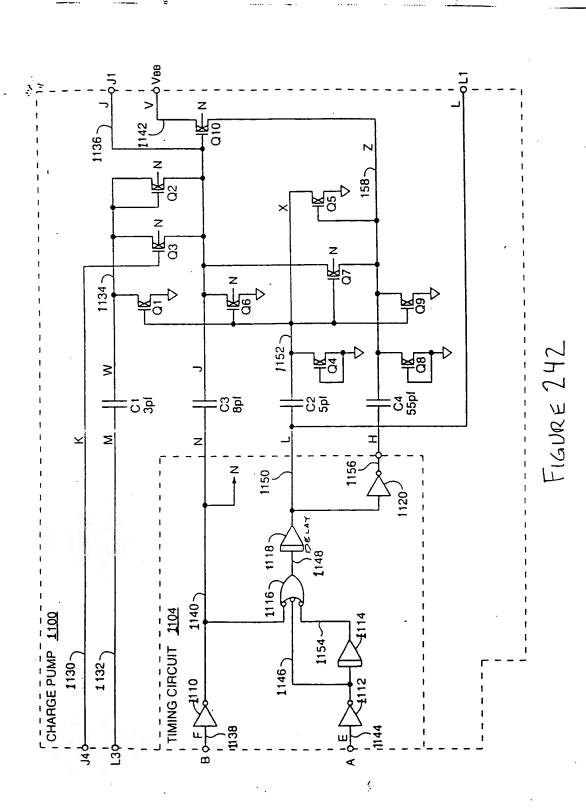
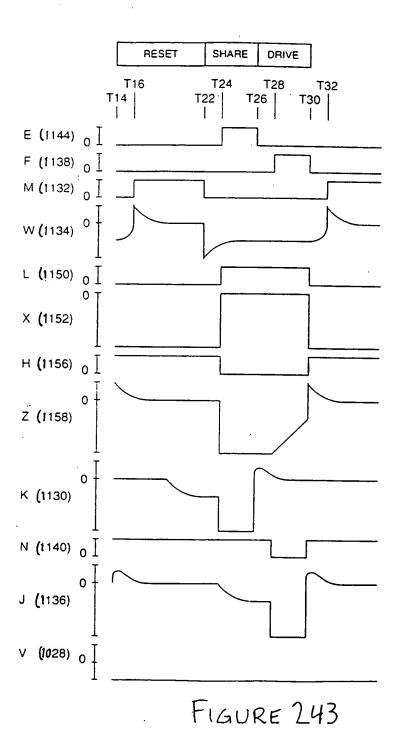


FIGURE 240







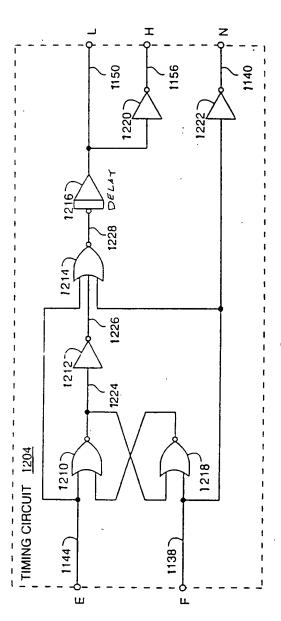


FIGURE 244

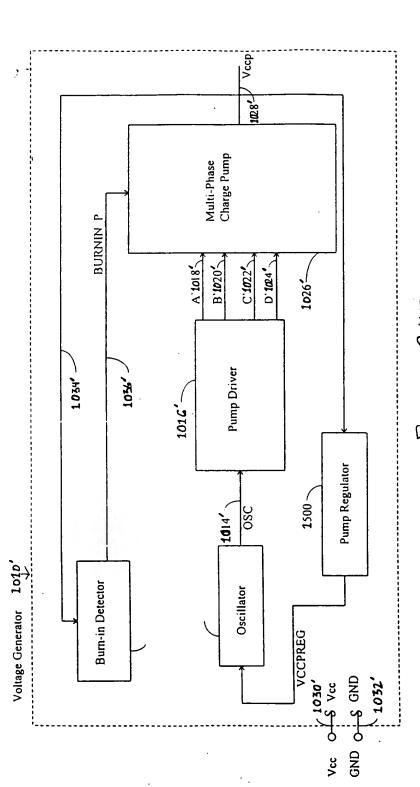
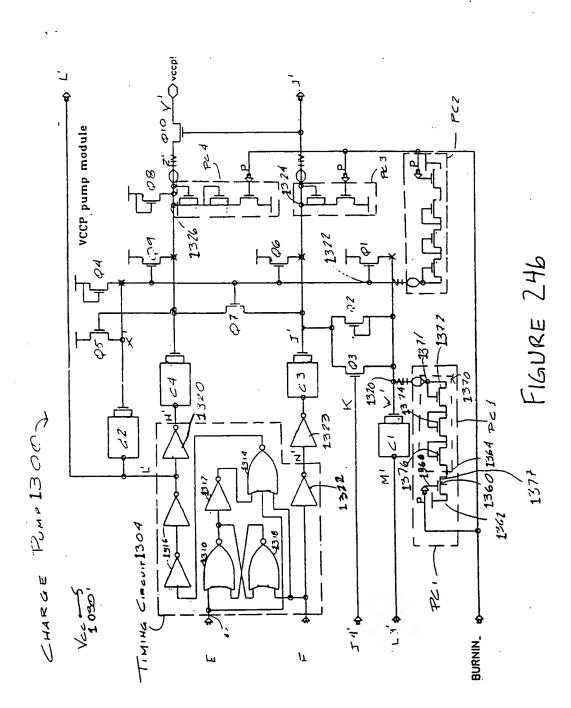


FIGURE 245



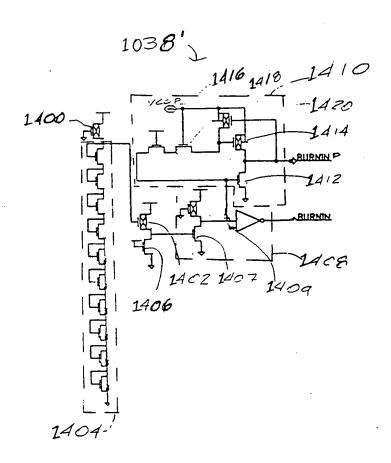


FIGURE 247

1500 1